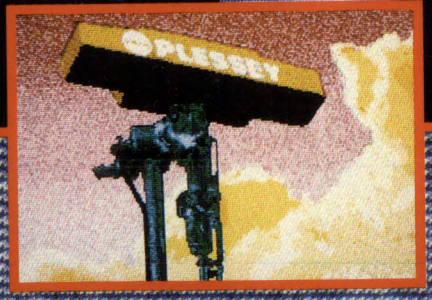
DIGITAL SIGNAL PROCESSING

IC Handbook



Plessey Semiconductors

DIGITAL SIGNAL PROCESSING

IC Handbook

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Foreword

The PDSP family of digital signal processing components are the first DSP building block parts to offer a significant increase in integration over the familiar multipliers, ALUs and Address Generators.

Despite the fact that the data in almost all DSP applications is complex-valued (i.e. of the form A + jB), the hardware of current DSP processors is only capable of operation on real data. This slows processing and complicates microcoding.

The PDSP family is the only DSP chip set to offer Complex Arithmetic as a standard feature. Systems configured around PDSP Complex Arithmetic elements offer 4-fold improvements in speed and substantial improvement in board area and power consumption.

Application areas covered by the PDSP family include:

Digital Filtering
Pulse Compression
Digital Modulation/Demodulation
FFT
Correlation/Convolution
Image Processing
High Speed Computation
Waveform Synthesis

Contents

Technical Data

PDSP1601/PDSP1601A

AUGMENTED ARITHMETIC LOGIC UNIT

(SUPERSEDES APRIL 1987 EDITION)

The PDSP1601 is a high performance 16-bit arithmetic logic unit with an independent on-chip 16-bit barrel shifter. The PDSP1601A has two operating modes giving 20MHz or 10MHz register-to-register transfer rates.

The PDSP1601 supports Multicycle multiprecision operation. This allows a single device to operate at 20MHz for 16-bit fields, 10MHz for 32-bit fields and 5MHz for 64-bit fields. The PDSP1601 can also be cascaded to produce wider words at the 20MHz rate using the Carry Out and Carry In pins. The Barrel Shifter is also capable of extension, for example the PDSP1601 can be used to select a 16-bit field from a 32-bit input in 100ns.

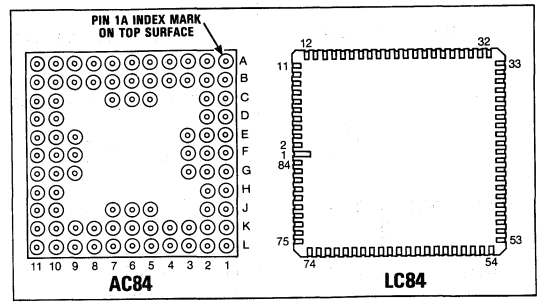


Fig.1 Pin connections - bottom view

PIN DESCRIPTIONS

LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function
1	C6	IA4	22	F3	GND	43	J6	IS0	64	F9	GND
2	A6	MSB	23	G3	MSA0	44	J7	IS1	65	F11	C8
3	A5	MSS	24	G1	MSA1	45	L7	IS2	66	E11	C9
4	B5	B15	25	G2	A15	46	K7	IS3	67	E10	C10
5	C5	B14	26	F1	A14	47	L6	SV0	68	E9	C11
6	A4	B13	27	H1	A13	48	L8	SV1	69	D11	C12
7	B4	B12	28	H2	A12	49	K8	SV2	70	D10	C13
8	A3	B11	29	J1	A11	50	L9	SV3	71	C11	C14
9	A2	B10	30	K1	A10	51	L10	$\overline{\text{SVOE}}$	72	B11	C15
10	B3	B9	31	J2	A9	52	K9	RS0	73	C10	$\overline{\text{OE}}$
11	A1	B8	32	L1	A8	53	L11	RS1	74	A11	BFP
12	B2	B7	33	K2	A7	54	K10	VCC	75	B10	VCC
13	C2	B6	34	K3	A6	55	J10	RS2	76	B9	CO
14	B1	B5	35	L2	A5	56	K11	C0	77	A10	RA0
15	C1	B4	36	L3	A4	57	J11	C1	78	A9	RA1
16	D2	B3	37	K4	A3	58	H10	C2	79	B8	RA2
17	D1	B2	38	L4	A2	59	H11	C3	80	A8	CI
18	E3	B1	39	J5	A1	60	F10	C4	81	B6	IA0
19	E2	B0	40	K5	A0	61	G10	C5	82	B7	IA1
20	E1	$\overline{\text{CEB}}$	41	L5	$\overline{\text{CEA}}$	62	G11	C6	83	A7	IA2
21	F2	CLK	42	K6	MSC	63	G9	C7	84	C7	IA3

FEATURES

- 16-bit, 32 Instruction 20MHz ALU
- 16-bit, 20MHz Logical, Arithmetic or Barrel Shifter
- Independent ALU and Shifter Operation
- 4 x 16-bit On Chip Scratchpad Registers
- Multiprecision Operation; e.g. 200ns 64-bit Accumulate
- Three Port Structure with Three Internal Feedback Paths Eliminates I/O Bottlenecks
- Block Floating Point Support
- 2-micron CMOS
- 300mW Maximum Power Dissipation
- 84-pin Pin Grid Array or 84 Contact LCC Packages

APPLICATIONS

- Digital Signal Processing
- Array Processing
- Graphics
- Database Addressing
- High Speed Arithmetic Processors

ASSOCIATED PRODUCTS

PDSP16112 Complex Multiplier
PDSP1640 40MHz Address Generator
PDSP16116 16 x 16 Complex Multiplier
PDSP16318 Complex Accumulator
PDSP16330 Pythagoras Processor

PIN DESCRIPTIONS

Symbol	Pin No. (LC84 Package)	Description
MSB	2	**ALU B-input multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
MSS	3	**Shifter Input multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
B15 - B0	4 - 19	**B Port data input**. Data presented to this port is latched into the input register on the rising edge of CLK. B15 is the MSB.
$\overline{CEB}$	20	**Clock enable, B Port input register**. When low the clock to this register is enabled.
CLK	21	**Common clock to all internal registered elements**. All registers are loaded, and outputs change on the rising edge of CLK.
MSA0 - MSA1	23 - 24	**ALU A-input multiplexer select control.**[1] These inputs are latched internally on the rising edge of CLK.
A15 - A0	25 - 40	**A Port data input**. Data presented to this port is latched into the input register on the rising edge of CLK. A15 is the MSB.
$\overline{CEA}$	41	**Clock enable, A Port input register**. When low the clock to this register is enabled.
MSC	42	**C-Port multiplexer select control.**[1] This input is latched internally on the rising edge of CLK.
IS0 - IS3	43 - 46	**Instruction inputs to Barrel Shifter, IS3 = MSB.**[1] These inputs are latched internally on the rising edge of CLK.
SV0 - SV3	47 - 50	**Shift Value I/O Port**. This port is used as an input when shift values are supplied from external sources, and as an output when Normalise operations are invoked. The I/O functions are determined by the IS0 - IS3 instruction inputs, and by the $\overline{SVOE}$ control. The shift value is latched internally on the rising edge of CLK.
$\overline{SVOE}$	51	**SV Output enable**. When high the SV port can only operate as an input. When low the SV port can act as an input or as an output, according to the IS0 - IS3 instruction. This pin should be tied high or low, depending upon the application.
RS0, RS1, RS2	52 - 53 55	**Instruction inputs to Barrel Shifter registers.**[1] These inputs are latched internally on the rising edge of CLK.
C0 - C15	56 - 63 65 - 72	**C Port data output**. Data output on this port is selected by the C output multiplexer. C15 is the MSB.
$\overline{OE}$	73	**Output enable**. The C Port outputs are in a high impedance condition when this control is high.
BFP	74	**Block Floating Point Flag** from ALU, active high.
CO	76	**Carry out** from MSB of ALU.
RA0 - RA2	77 - 79	**Instruction inputs to ALU registers.**[1] These inputs are latched internally on the rising edge of CLK.
CI	80	**Carry in** to LSB of ALU.
IA0 - IA3 IA4	81 - 84 1	**Instruction inputs to ALU,**[1] IA4 = MSB. These inputs are latched internally on the rising edge of CLK.
Vcc	54 & 75	**+5V supply**. Both Vcc pins must be connected
GND	22 & 64	**0V supply**. Both GND pins must be connected.

NOTES
1. All instructions are executed in the cycle commencing with the rising edge of the CLK which latches the inputs.

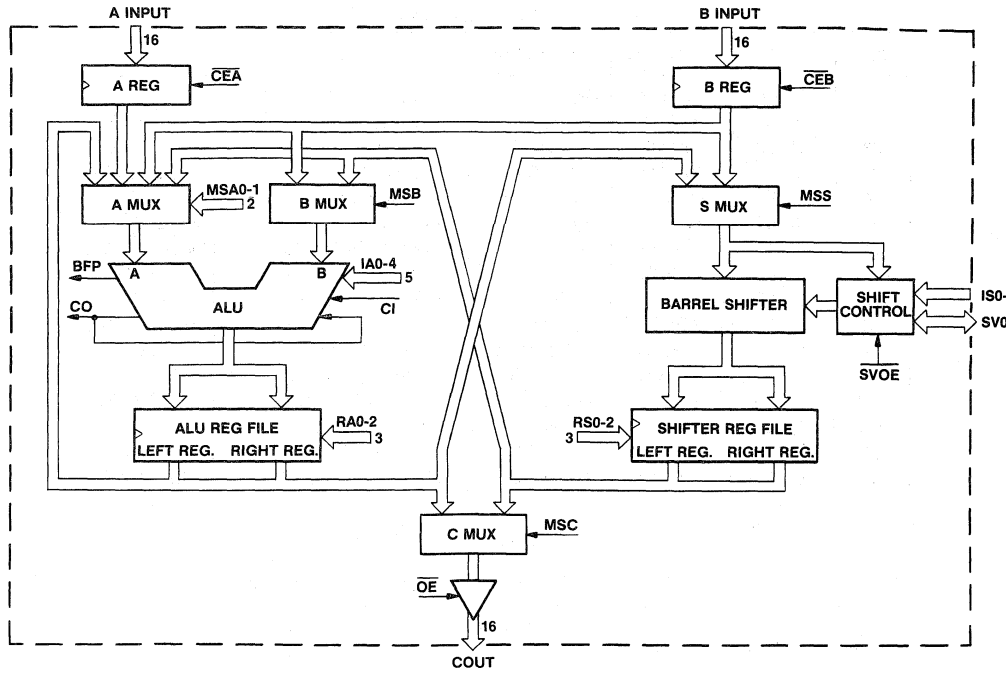


Fig.2 PDSP1601 block diagram

FUNCTIONAL DESCRIPTION

The PDSP1601 contains four main blocks: the ALU, the Barrel Shifter and the two Register Files.

The ALU

The ALU supports 32 instructions as detailed in Table 1.

The inputs to the ALU are selected by the A and B MUXs. Data will fall through from the selected register through the A or B input MUXs and the ALU to the ALU output register file in 50ns for the PDSP1601A (100ns for the PDSP1601).

The ALU instructions are latched, such that the instruction will not start executing until the rising edge of CLK latches the instruction into the device.

The ALU accepts a carry in from the CI input and supplies a carry out to the CO output. Additionally, at the end of each cycle, the carry out from the ALU is loaded into an internal 1 bit register, so that it is available as an input to the ALU on the next cycle. In this manner, multicycle, multiprecision operations are supported. (See MULTICYCLE CASCADE OPERATIONS).

BFP Flag

The ALU has a user programmable BFP flag. This flag may be programmed to become active at any one of four conditions. Two of these conditions are intended to support Block Floating Point operations, in that they provide flags indicating that the ALU result is within a factor of two or four of overflowing the 16 bit number range. For multiprecision operations the flag is only valid whilst the most significant 16 bit byte is being processed. In this manner the BFP flag may be used over any extended word width.

The remaining two conditions detect either an overflow condition or a zero result. For the overflow condition to be active the ALU result must have overflowed into the 16th (sign) bit, (this flag is only valid whilst the most significant 16 bit byte is being processed). The zero condition is active if the result from the ALU is equal to zero. For multiprecision operations the zero flag must be active for all of the 16 bit bytes of an extended word.

The BFP flag is programmed by executing one of the four SBFXX instructions (see Table 1). During the execution of any of these four instructions, the output of the ALU is forced to zero.

Multicycle/Cascade Operation

The ALU arithmetic instructions contain two or three options for each arithmetic operation.

The ALU is designed to operate with two's complement arithmetic, requiring a one to be added to the LSB for all subtract operations. The instructions set includes instructions that will force a one into the LSB, e.g. MIAX1, AMBX1, BMAX1 (see Table 1).

These instructions are used for the least significant 16 bit byte of any subtract operation.

The user has the option of cascading multiple devices, or multicycling a single device to extend the arithmetic precision. Should the user cascade multiple devices, then the cascade arithmetic instructions using the external CI input should be employed for all but the least significant 16 bit byte, e.g. MIACI, APBCI, BMACI (see Table 1).

Should the user multicycle a single device, then the Multicycle Arithmetic instructions, using the internally registered CO bit should be employed for all but the least significant 16 bit byte, e.g. MIACO, APBCO, AMBCO, BMACO (see Table 1).

Table 1 ALU instructions

1a. ARITHMETIC INSTRUCTIONS

Inst	IA4-AI0	Mnemonic	Operation	Function	Mode
00	00000	CLRXX	RESET	CLEAR ALL REGISTERS	------
01	00001	MIAX1	MINUS A	NA Plus 1	LSBYTE
02	00010	MIACI	MINUS A	NA Plus CI	CASCADE
03	00011	MIACO	MINUS A	NA Plus CO	MULTICYCLE
04	00100	A2SGN	A/2	A/2 Sign Extend	MSBYTE
05	00101	A2RAL	A/2	A/2 with RAL LSB	MULTICYCLE
06	00110	A2RAR	A/2	A/2 with RAR LSB	MULTICYCLE
07	00111	A2RSX	A/2	A/2 with RSX LSB	MULTICYCLE
08	01000	APBCI	A PLUS B	A Plus B Plus CI	CASCADE
09	01001	APBCO	A PLUS B	A Plus B Plus CO	MULTICYCLE
0A	01010	AMBX1	A MINUS B	A Plus NB Plus 1	LSBYTE
0B	01011	AMBCI	A MINUS B	A Plus NB Plus CI	CASCADE
0C	01100	AMBCO	A MINUS B	A Plus NB Plus CO	MULTICYCLE
0D	01101	BMAX1	B MINUS A	NA Plus B Plus 1	LSBYTE
0E	01110	BMACI	B MINUS A	NA Plus B Plus CI	CASCADE
0F	01111	BMACO	B MINUS A	NA Plus B Plus CO	MULTICYCLE

1b. LOGICAL INSTRUCTIONS

Inst	IA4-IA0	Mnemonic	Operation	Function
10	10000	ANXAB	A AND B	A.B
11	10001	ANANB	A AND NB	A.NB
12	10010	ANNAB	NA AND B	NA.B
13	10011	ORXAB	A OR B	A + B
14	10100	ORNAB	NA OR B	NA + B
15	10101	XORAB	A XOR B	A XOR B
16	10110	PASXA	PASS A	A
17	10111	PASNA	INVERT A	NA

1c. CONTROL INSTRUCTIONS

Inst	IA4-IA0	Mnemonic	Operation
18	11000	SBFOV	Set BFP Flag to OVR, Force ALU output to zero
19	11001	SBFU1	Set BFP Flag to UND 1 Force ALU output to zero
1A	11010	SBFU2	Set BFP Flag to UND 2 Force ALU output to zero
1B	11011	SBFZE	Set BFP Flag to ZERO Force ALU output to zero
1C	11100	OPONE	Output 0001 Hex
1D	11101	OPBYT	Output 00FF Hex
1E	11110	OPNIB	Output 000F Hex
1F	11111	OPALT	Output 5555 Hex

KEY

A = A Input to ALU
B = B Input to ALU
CI = External Carry in to ALU
CO = Internally Registered Carry out from ALU
RAL = ALU Register (Left)
RAR = ALU Register (Right)
RSX = Shifter Register (Left or Right)

MNEMONICS

CLRXX	Clear All Registers to zero		
MIAXX	Minus A,	XX	= Carry in to LSB
A2XXX	A Divided by 2,	XXX	= Source of MSB
APBXX	A Plus B,	XX	= Carry in to LSB
AMBXX	A Minus B,	XX	= Carry in to LSB
BMAXX	B Minus A,	XX	= Carry in to LSB
ANX-Y	AND	X	= Operand 1, Y = Operand 2
ORX-Y	OR	X	= Operand 1, Y = Operand 2
XORXY	Exclusive OR	X	= Operand 1, Y = Operand 2
PASXX	Pass	XX	= Operand
SBFXX	Set BFP Flag	XX	= Function
OPXXX	Output Constant	XXX	= Value

Divide by Two

The ALU has four (A2SGN, A2RAL, A2RAR, A2RSX) instructions used for right shifting (dividing by two) extended precision words. These words, (up to 64 bits) may be stored in the two on-chip register files. When the least significant 16 bit word is shifted, the vacant MSB must be filled with the LSB from the next most significant 16 bit byte. This is achieved via the A2RAL, A2RAR or A2RSX instructions which indicate the source of the new MSB (see ALU INSTRUCTION SET).

When the most significant 16 bit byte is right shifted, the MSB must be filled with a duplicate of the original MSB so as to maintain the correct sign (Sign Extension). This operation is achieved via the A2SGN instruction (see Table 1).

Constants

The ALU has four instructions (OPONE, OPBYT, OPNIB, OPALT) that force a constant value onto the ALU output. These values are primarily intended to be used as masks, or the seeds for mask generation, for example, the OPONE instruction will set a single bit in the least significant position. This bit may be rotated any where in the 16 bit field by the Barrel Shifter, allowing the AND function of the ALU to perform bit-pick operations on input data.

CLR

The ALU instruction CLRXX is used as a Master Reset for the entire device. This instruction has the effect of:

1. Clearing ALU and Barrel Shifter register files to zero.
2. Clearing A and B port input registers to zero.
3. Clearing the R1 and R2 shift control registers to zero.
4. Clearing the internally registered CO bit to zero.
5. Programming the BFP flag to detect *overflow* conditions.

The Barrel Shifter

The Barrel Shifter supports 16 instructions as detailed in Table 2. The input to the Barrel Shifter is selected by the S MUX. Data will fall through from the selected register, through the S MUX and the Barrel Shifter to the shifter output register file in 50ns for the PDSP1601A (100ns for the PDSP1601).

The Barrel Shifter instructions are latched, such that the instructions will not start executing until the rising edge of CLK latches the instruction into the device.

The Barrel Shifter is capable of Logical Arithmetic or Barrel Shifts in either direction.

A. Logical shifts discard bits that exit the 16 bit field and fill spaces with zeros.
B. Arithmetic shifts discard bits that exit the 16 bit field and fill spaces with duplicates of the original MSB.
C. Barrel Shifts rotate the 16 bit fields such that bits that exit the 16 bit field to the left or right reappear in the vacant spaces on the right or left.

The amount of shift applied is encoded onto the 4 bit Barrel Shifter input as illustrated in Table 3. The type of shift and the amount are determined by the shift control block. The shift control block (see Fig.3) accepts and decodes the four bit IS0-3 instruction. The shift control block contains a priority encoder and two, user programmable 4 bit registers R1 and R2.

There are four possible sources of shift value that can be passed onto the Barrel Shifter, these are:

1. The Priority Encoder
2. The SV input
3. The R1 register
4. The R2 register

Inst	IS3-IS0	Mnemonic	Function	I/O
0	0000	LSRSV	Logical Shift Right by SV	I
1	0001	LSLSV	Logical Shift Left by SV	I
2	0010	BSRSV	Barrel Shift Right by SV	I
3	0011	BSLSV	Barrel Shift Left by SV	I
4	0100	LSRR1	Logical Shift Right by R1	X
5	0101	LSLR1	Logical Shift Left by R1	X
6	0110	LSRR2	Logical Shift Right by R2	X
7	0111	LSLR2	Logical Shift Left by R2	X
8	1000	LR1SV	Load Register 1 From SV	I
9	1001	LR2SV	Load Register 2 From SV	I
A	1010	ASRSV	Arithmetic Shift Right by SV	I
B	1011	ASRR1	Arithmetic Shift Right by R1	X
C	1100	ASRR2	Arithmetic Shift Right by R2	X
D	1101	NRMXX	Normalise Output PE	O
E	1110	NRMR1	Normalise Output PE, Load R1	O
F	1111	NRMR2	Normalise Output PE, Load R2	O

Table 2 Barrel shifter instructions

KEY

SV = Shift Value
R1 = Register 1
R2 = Register 2
PE = Priority Encoder Output
I => SV Port operates as an Input
O => SV Port operates as an Output
X => SV Port in a High Impedance State

MNEMONICS

LSXYY Logical Shift, X = Direction YY = Source of Shift Value
BSXYY Barrel Shift, X = Direction YY = Source of Shift Value
ASXYY Arithmetic Shift, X = Direction YY = Source of Shift Value
LXXYY Load XX = Target YY = Source
NRMYY Normalise by PE, Output PE value on SV Port, Load YY Reg

SV3	SV2	SV1	SV0	Shift
0	0	0	0	No shift
0	0	0	1	1 place
0	0	1	0	2 places
0	0	1	1	3 places
0	1	0	0	4 places
0	1	0	1	5 places
0	1	1	0	6 places
0	1	1	1	7 places
1	0	0	0	8 places
1	0	0	1	9 places
1	0	1	0	10 places
1	0	1	1	11 places
1	1	0	0	12 places
1	1	0	1	13 places
1	1	1	0	14 places
1	1	1	1	15 places

Table 3 Barrel shifter codes

Priority Encoder

If the priority encoder is selected as the source of the shift value (instructions:- NRMXX, NRMR1, MRMRZ), then within one 100ns cycle or two 50ns cycles for the PDSP1601A (one 200ns or two 100ns cycles for the PDSP1601), the shift circuitry will:

(1) Priority encode the 16 bit input to the Barrel Shifter and place the 4 bit value in either of the R1 or R2 registers and output the value on the SV port (if enabled by $\overline{\text{SVOE}}$).

(2) Shift the 16 bit input by the amount indicated by the Priority Encoder such that the output from the Barrel Shifter is a normalised value.

SV Input

If the SV port is selected as the source of the shift value, then the input to the Barrel Shifter is shifted by the value stored in the internal SV register.

$\overline{\text{SVOE}}$

The SV port acts as an input or an output depending upon the IS0-3 instruction. If the user does not wish to use the normalise instructions, then the SV port may be forced to be input only by tying the $\overline{\text{SVOE}}$ control high. In this mode the SV port may be considered an extension of the instruction inputs.

R1 and R2 Registers

The R1 and R2 registers may be loaded from the Priority Encoder (NRMR1 and NRMR2) or from the SV input (LR1SV, LR2SV).

Whilst the latter two instructions are executing, the Barrel Shifter will pass its input to the output unshifted.

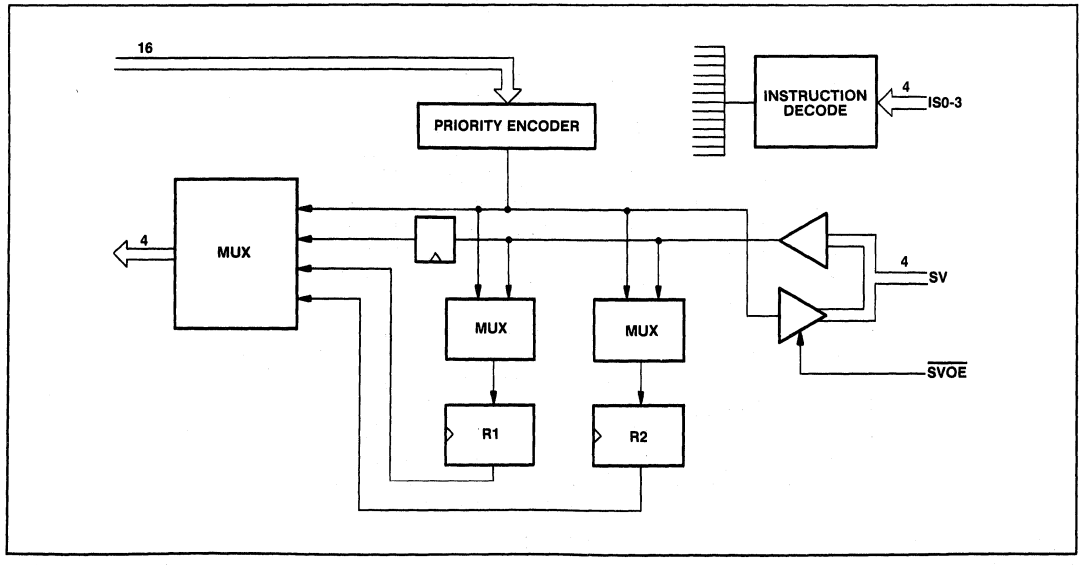


Fig.3 Shift control block

The Register Files

There are two on-chip register files (ALU and Shifter), each containing two 16 bit registers and each supporting 8 instructions (see Table 4). The instructions for the ALU register file and the Barrel Shifter Register file are the same.

The Inputs to the register files come from either the ALU or the Barrel Shifter, and are loaded into the Register files on the rising edge of CLK.

The register file instructions are latched such that the instruction will not start executing until the rising edge of the CLK latches the instruction into the device.

The register file instructions (see Table 4) allow input data to be loaded into either, neither or both of the registers. Data is loaded at the end of the cycle in which the instruction is executing.

The register file instructions allow the output to be sourced from either of the two registers, the selected output will be valid during the cycle in which the instruction is executing.

ALU REGISTER INSTRUCTIONS			
Inst	**RA2-RA0**	**Mnemonic**	**Operation**
0	000	LLRRR	Load Left Reg Output Right Reg
1	001	LRRLR	Load Right Reg Output Left Reg
2	010	LLRLR	Load Left Register, Output Left Reg
3	011	LRRRR	Load Right Register, Output Right Reg
4	100	LBRLR	Load Both Registers, Output Left Reg
5	101	NOPRR	No Load Operation, Output Right Reg
6	110	NOPLR	No Load Operation, Output Left Reg
7	111	NOPPS	No Load Operation, Pass ALU Result
SHIFTER REGISTER INSTRUCTIONS			
Inst	**RS2-RS0**	**Mnemonic**	**Operation**
0	000	LLRRR	Load Left Reg Output Right Reg
1	001	LRRLR	Load Right Reg Output Left Reg
2	010	LLRLR	Load Left Register, Output Left Reg
3	011	LRRRR	Load Right Register, Output Right Reg
4	100	LBRLR	Load Both Registers, Output Left Reg
5	101	NOPRR	No Load Operation, Output Right Reg
6	110	NOPLR	No Load Operation, Output Left Reg
7	111	NOPPS	No Load Operation, Pass Barrel Shifter Result

Table 4 ALU and shift register instructions mnemonics

MNEMONICS

LXXYY	Load XX = Target,	YY	= Source of Output
LBOXX	Load Both Registers,	XX	= Source of Output
NOPXX	No Load Operation,	XX	= Source of Output

Multiplexers

There are four user selectable on-chip multiplexers (A-MUX, B-MUX, S-MUX and C-MUX).

These four multiplexers support instructions as tabulated in Table 5.

The MUX instructions are latched such that the instruction will not start executing until the rising edge of CLK latches the instruction onto the device.

		MSA1	MSA0	Output
A-MUX	MARAX	0	0	ALU REGISTER FILE OUTPUT
	MAAPR	0	1	A-PORT INPUT
	MABPR	1	0	B-PORT INPUT
	MARSX	1	1	SHIFTER REGISTER FILE OUTPUT

	MSB	Output
B-MUX	0	B-PORT INPUT
	1	SHIFTER REGISTER FILE OUTPUT

	MSS	Output
S-MUX	0	B-PORT INPUT
	1	ALU REGISTER FILE OUTPUT

	MSC	Output
C-MUX	0	ALU REGISTER FILE OUTPUT
	1	SHIFTER REGISTER FILE OUTPUT

Table 5

INSTRUCTION SET

ALU Arithmetic Instructions

Mnemonic	Op Code	Function
CLRXX	<00>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the A Port, B Port, ALU, Barrel Shifter, and Shift Control Registers will be loaded with zeros. The internal registered CO will also be set to zero, and the BFP flag will be set to activate on overflow conditions.
MIAX1	<01>	The A input to the ALU is inverted and a one is added to the LSB.
MIACI	<02>	The A input to the ALU is inverted and the CI input is added to the LSB.
MIACO	<03>	The A input to the ALU is inverted and the CO output from the ALU on the previous cycle is added to the LSB.
A2SGN	<04>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled by duplicating the original MSB (Sign Extension).
A2RAL	<05>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the ALU left register.
A2RAR	<06>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the ALU right register.
A2RSX	<07>	The A input to the ALU is right shifted one bit position. The LSB is discarded, and the vacant MSB is filled with the LSB from the B input to the ALU.
APBCI	<08>	The A input to the ALU is added to the B input, and the CI input is added to the LSB.
APBCO	<09>	The A input to the ALU is added to the B input, and the CO out from the ALU on the previous cycle is added to the LSB.
AMBX1	<0A>	The A input to the ALU is added to the inverted B input, and a one is added to the LSB.
AMBCI	<0B>	The A input to the ALU is added to the inverted B input, and the CI input is added to the LSB.
AMBCO	<0C>	The A input to the ALU is added to the inverted B input, and the CO out from the ALU on the previous cycle is added to the LSB.
BMAX1	<0D>	The inverted A input to the ALU is added to the B input, and a one is added to the LSB.
BMACI	<0E>	The inverted A input to the ALU is added to the B input, and the CI input is added to the LSB.
BMACO	<0F>	The inverted A input to the ALU is added to the B input, and the CO out from the ALU on the previous cycle is added to the LSB.

ALU Logical Instructions

Mnemonic	Op Code	Function
ANXAB	<10>	The A input to the ALU is logically 'ANDed' with the B input.
ANANB	<11>	The A input to the ALU is logically 'ANDed' with the inverse of the B input.
ANNAB	<12>	The inverse of the A input to the ALU is logically 'ANDed' with the B input.
ORXAB	<13>	The A input to the ALU is logically 'ORed' with the B input.
ORNAB	<14>	The inverse of the A input to the ALU is logically 'ORed' with the B input.
XORAB	<15>	The A input to the ALU is logically Exclusive-ORed with the B input.
PASXA	<16>	The A input to the ALU is passed to the output.
PASNA	<17>	The inverse of the A input to the ALU is passed to the output.

ALU Control Instructions

Mnemonic	Op Code	Function
SBFOV	<18>	The BFP flag is programmed to activate when an ALU operation causes an overflow of the 16 bit number range. This flag is logically the exclusive-or of the carry into and out of the MSB of the ALU. For the most significant Byte this flag indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFU1	<19>	The BFP flag is programmed to activate when an ALU operation comes within a factor of two of causing an overflow of the 16 bit number range. For the most signficant Byte this flag indicates that the result of an arithmetic two's complement operation is within a factor of two of overflowing into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFU2	<1A>	The BFP flag is programmed to activate when an ALU operation comes within a factor of four of causing an overflow of the 16 bit number range. For the most significant Byte this flag indicates that the result of an arithmetic two's complement operation is within a factor of four of overflowing into the sign bit. The output of the ALU is forced to zero for the duration of this instruction.
SBFZE	<1B>	The BFP flag is programmed to activate when an ALU operation causes a result of zero. The output of the ALU is forced to zero for the duration of this instruction. During the execution of this instruction the BFP flag will become active.
OPONE	<1C>	The ALU will output the binary value 0000000000000001, the MSB on the left.
OPBYT	<1D>	The ALU will output the binary value 0000000011111111, the MSB on the left.
OPNIB	<1E>	The ALU will output the binary value 0000000000001111, the MSB on the left.
OPALT	<1F>	The ALU will output the binary value 0101010101010101, the MSB on the left.

Barrel Shifter Instructions

Mnemonic	Op Code	Function
LSRSV	<0>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs are discarded, and the vacant MSBs are filled with zeros.
LSLSV	<1>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The MSBs are discarded, and the vacant LSBs are filled with zeros.
BSRSV	<2>	The 16 bit input to the Barrel Shifter is rotated to the right by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs that exit the 16 bit field to the right, reappear in the vacant MSBs on the left.
BSLSV	<3>	The 16 bit input to the Barrel Shifter is rotated to the left by the number of places indicated by the magnitude of the four bit number present in the SV register. The MSBs that exit the 16 bit field to the left, reappear in the vacant LSBs on the right.
LSRR1	<4>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The LSBs are discarded, and the vacant MSBs are filled with zeros.
LSLR1	<5>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The MSBs are discarded, and the vacant LSBs are filled with zeros.
LSRR2	<6>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The LSBs are discarded, and the vacant MSBs are filled with zeros.
LSLR2	<7>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The MSBs are discarded, and the vacant LSBs are filled with zeros.

Mnemonic	Op Code	Function
LR1SV	<8>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the R1 register will be loaded with the data present on the SV port. The input to the Barrel Shifter will be passed onto the output unshifted.
LR2SV	<9>	On the rising edge of CLK at the end of the cycle in which this instruction is executing, the R2 register will be loaded with the data present on the SV port. The input to the Barrel Shifter will be passed onto the output unshifted.
ASRSV	<A>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number present in the SV register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
ASRR1	<B>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R1 register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
ASRR2	<C>	The 16 bit input to the Barrel Shifter is right shifted by the number of places indicated by the magnitude of the four bit number resident within the R2 register. The LSBs are discarded, and the vacant MSBs are filled with duplicates of the original MSB. (Sign Extension).
NRMXX	<D>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is also output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.
NRMR1	<E>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is loaded into the R1 register at the end of the cycle, and is also output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.
NRMR2	<F>	The 16 bit input to the Barrel Shifter is left shifted by the number of places indicated by the magnitude of the four bit number output from the Priority Encoder. This value is loaded into the R2 register at the end of the cycle, and also output on the SV port (provided $\overline{SVOE}$ is low). The effect of this operation is to left shift the input by the necessary amount (max 15 places) to result in the MSB and the next most significant bit being different. This has the effect of eliminating unnecessary Sign Bits, and hence Normalising the input data. The MSBs shifted out to the left are discarded, and the vacant LSBs on the right are filled with zeros.

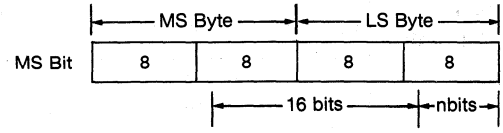
Barrel Shifter or ALU Register Instructions

Mnemonic	Op Code	Function
LLRRR	<0>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Right register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Left Register.
LRRLR	<1>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Right Register.
LLRLR	<2>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Left Register.
LRRRR	<3>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed,the contents of the Right register will appear on the output.On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into the Right Register.
LBRLR	<4>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle, the data on the register inputs will be loaded into both Left and Right Registers.
NOPRR	<5>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Right register will appear on the output. On the rising edge ofd CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.
NOPLR	<6>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the contents of the Left register will appear on the output. On the rising edge of CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.
NOPPS	<7>	After the rising edge of CLK at the beginning of the cycle in which this instruction is executed, the input to the registers will appear on the output. On the rising edge of CLK at the end of the cycle no load operation will occur, the register contents will remain unchanged.

TYPICAL APPLICATION

Select a 16 bit field from each word in a block of 32 bit words with a 10MHz throughput.

The 16 bit field indicated is to be selected from each 32 bit word.



The 32 bit words are fed into the B port of the PDSP1601 in two cycles, MS byte first.

The PDSP1601 shift control is initiated by programming the R1 and R2 registers with n and 16-n respectively.

The shift operation is implemented in three steps:-

(1) The MS byte is logically left shifted (16-n) places, the MSBs being discarded and the LSB spaces being filled with zeros. This shifted data is loaded into the shifter register file left register.

(2) The LS byte is logically right shifted, n-places, the LSBs being discarded and the MSBs being filled with zeros. This shifted data is loaded into the shifter register file left register.

During this cycle the previous contents of this register are passed through the ALU to the ALU register file left register.

(3) While the MS byte of the next 32 bit word is shifted in the Barrel Shifter, the two previous results, resident within the left registers of the ALU and Shifter Register files are 'ORed' by the ALU, the result being the desired 16 bit field is loaded into the ALU register file right register ready to be output on the next cycle.

The instructions from initialisation are given in Table 6.

CLK	CEB	MSA	MSB	MSS	MSC	IA	IS	SV	RA	RS	Comment
1/	1	MARSX	1	0	0	CLRXX	X	X	NOPLR	NOPLR	Clear
2/	1	MARSX	1	0	0	PASXA	LR1SV	n	NOPLR	NOPLR	Load R1 with n
3/	0	MARSX	1	0	0	PASXA	LR2SV	(16-n)	NOPLR	NOPLR	Load R2 with (16-n)
4/	0	MARSX	1	0	0	PASXA	LSLR2	X	NOPLR	LLRLR	Shift 1st MS byte
5/	0	MARSX	1	0	0	PASXA	LSRR1	X	LLRRR	LLRLR	Shift 1st LS byte
6/	0	MARAX	1	0	0	ORXAB	LSLR2	X	LRRLR	LLRLR	OR 1st bytes and shift 2nd MS byte
7/	0	MARSX	1	0	0	PASXA	LSRR1	X	LLRRR	LLRLR	Shift 2nd LS byte and output first result
8/	0	MARAX	1	0	0	ORXAB	LSLR2	X	LRRLR	LLRLR	Shift 3rd LS byte

Repeat instruction pair 5/ and 6/ until all 16 bit fields have been selected.

Table 6

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{CC}	-0.5 to 7.0V
Input Voltage V_{in}	-0.9 to V_{CC} +0.9V
Output Voltage V_{out}	-0.9 to V_{CC} +0.9V
Clamp diode current per pin Ik (See Note 2)	±18mA
Static discharge voltage (HMB)	500V
Storage temperature Ts	-65° C to +150° C
Ambient temperature with power applied T_{amb}	
Military	-40°C to +125°C
Industrial	-40°C to +85°C
Package power dissipation P_{TOT}	
AC	1000mW
LC	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C V_{CC} = 5.0V ± 10% Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	I_{OH} = 8mA
Output low voltage	V_{OL}			0.4	V	I_{OL} = -8mA
Input high voltage	V_{IH}	2.0			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	I_{IL}	-10		+10	μA	GND < V_{IN} < V_{CC}
V_{CC} current	I_{CC}			60	mA	T_{amb} = -40°C to +85°C
Output leakage current	I_{OZ}	-50		+50	μA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{OS}	15		80	mA	V_{CC} = Max
Input capacitance	C_{IN}		5		pF	

Switching Characteristics

Characteristic	Value				Units	Conditions
	PDSP1601		PDSP1601A			
	Min.	Max.	Min.	Max.		
CLK rising edge to C-PORT		40		25	ns	2 x LSTTL +20pF
CLK rising edge to CO		100		50	ns	1 x LSTTL +5pF
CLK rising edge to BFP		100		50	ns	1 x LSTTL +5pF
Setup $\overline{CEA}$ or $\overline{CEB}$ to CLK rising edge	30		15		ns	
Hold $\overline{CEA}$ or $\overline{CEB}$ to CLK rising edge		0		0	ns	
Setup A or B port inputs to CLK rising edge	40		20		ns	
Hold A or B port inputs to CLK rising edge		0		0	ns	
Setup MSA0-1, MSB, MSS, MSC, RA0-2	40		20		ns	
RS0-2, IA0-4, IS0-3 to CLK rising edge					ns	
Hold RS0-2, IA0-4, IS0-3 to CLK rising edge		0		0	ns	
Setup SV to CLK rising edge	40		20		ns	Input mode
Hold SV to CLK rising edge		0		0	ns	Input mode
CLK rising edge to SV		100		50	ns	20pF load
						SV o/p mode
$\overline{OE}$ ⌐ C-PORT ¬ Z					ns	2 x LSTTL +20pF
$\overline{OE}$ ⌐ C-PORT ⌐ Z					ns	2 x LSTTL +20pF
$\overline{OE}$ ¬ C-PORT Z ⌐					ns	2 x LSTTL +20pF
$\overline{OE}$ ¬ C-PORT Z ¬					ns	2 x LSTTL +20pF
Clock period (ALU & Barrel Shifter, serial mode)	200		100		ns	
Clock period (ALU & Barrel Shifter, parallel mode)	100		50		ns	
Clock high time	40		20		ns	
Clock low time	40		20		ns	

ORDERING INFORMATION

Industrial

PDSP1601 B0 AC
PDSP1601A B0 AC
PDSP1601 B0 LC
PDSP1601A B0 LC

Military

PDSP1601 A0 AC
PDSP1601A0 LC

Call for availability on High Reliability parts and MIL-883C screening.

PLESSEY
Semiconductors

PDSP1640/PDSP1640A

40MHz ADDRESS GENERATOR

(SUPERSEDES OCTOBER 1987 EDITION)

The PDSP1640/PDSP1640A is an 8-bit address generator which will cascade efficiently to wider address fields at very high speed, without the need for external carry logic.

Three PDSP1640As allow 24-bit addresses to be generated at up to 20MHz, four allow 32-bit addressing at up to 15MHz. A single PDSP1640A will address an 8-bit field at 40MHz.

FEATURES

- 40MHz 8-Bit Address Generator (PDSP1640A)
- Fast Cascade Logic gives 20MHz Operation at 24 Bits (PDSP1640A)
- Five On-Chip, User-Programmable Registers
- Output Mask Logic
- 2 micron CMOS
- 300mW Maximum Power Dissipation
- 28 Pin DIL, LCC or HC Package

APPLICATIONS

- DSP Address Generation
- Database Addressing
- DMA Controllers
- Modulo Counting

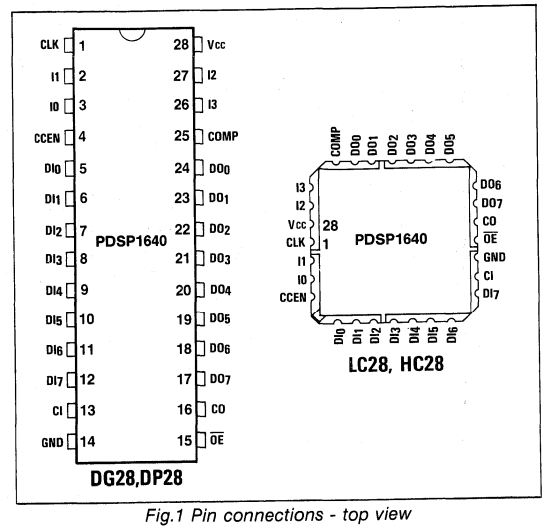


Fig.1 Pin connections - top view

ASSOCIATED PRODUCTS

PDSP16318 Complex Accumulator
PDSP16112 Complex Number Multiplier
PDSP1601 Arithmetic Logic Unit

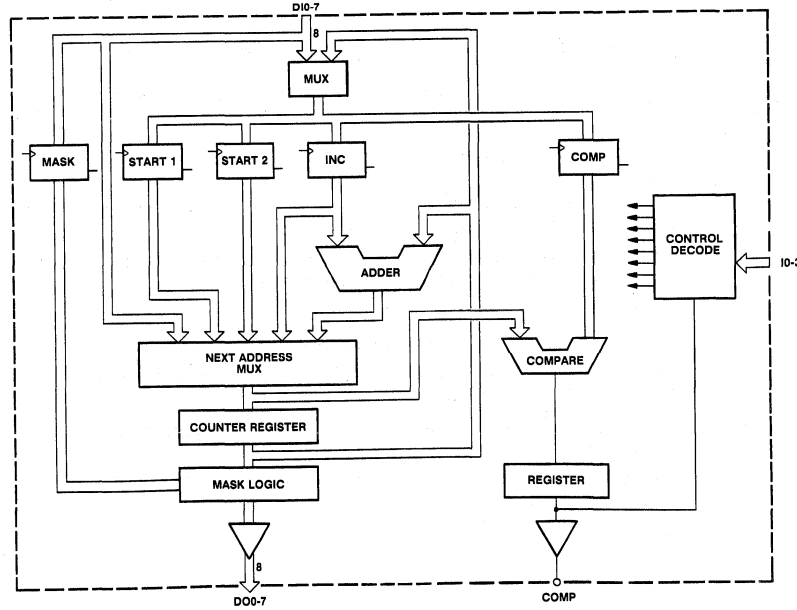


Fig.2 PDSP1640 simplified block diagram

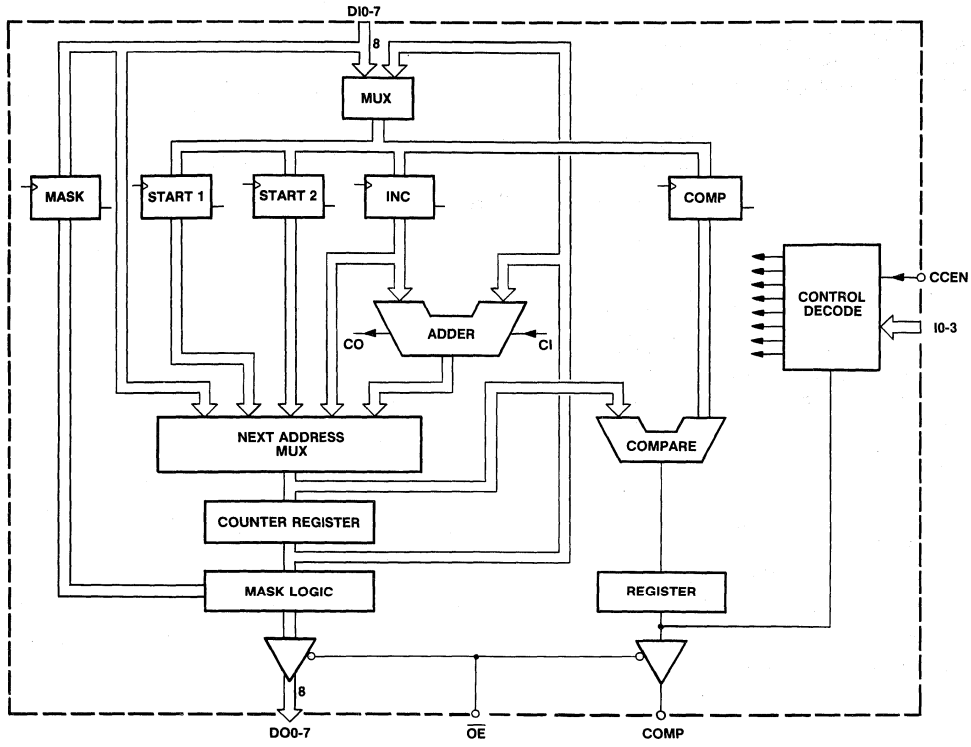


Fig.3 PDSP1640 block diagram

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
CLK	1	**Common clock** to all registered internal elements. All registers are loaded, and outputs change on the rising edge of CLK.
I0-3	3,2, 27,26	**Instruction inputs.** The 16 instructions executable by the PDSP1640 are encoded onto these four lines. The instruction for any cycle must be valid at the inputs prior to the rising edge of CLK defining the start of the cycle in which the instruction is to be executed. The I0-3 inputs are internally latched by the rising edge of CLK.
CCEN	4	**Conditional Instruction Enable.** The Conditional Instructions during the current cycle are enabled if CCEN goes high before the end of the cycle. CCEN may be controlled directly by microcode or, where multiple 1640's are used, this input is used for expansion. See Figs.6 and 7.
COMP	25	**Comparator Flag Output.** This indicates that the comparator has detected an 'equal to' condition, COMP changes when CLK goes HIGH.
CI	13	**Carry In.** Carry in to least significant bit of the 8-bit adder.
CO	16	**Carry Out.** Carry out from the MSB of the adder.
DI0-7	5-12	**Data Inputs.** 8-bit data input to PDSP1640. The data on this port is loaded into the on-board registers on the rising edge of CLK.
DO0-7	24-17	**Data Outputs.** The 8-bit output from the counter. The output changes on the rising edge of CLK.
$\overline{OE}$	15	**3-State Output Control.** When high, this signal forces the DO0-7 and COMP outputs into a high-impedance state.
GND	14	0V supply.
V_{CC}	28	+5V supply.

FUNCTIONAL DESCRIPTION

The PDSP1640 contains six main blocks; the five user programmable registers, an 8-bit Adder, the Mask Logic, a Comparator, the Control Decoder and the Next Address MUX and Counter Register.

The Registers

There are five user programmable registers; MASK, START1, START2, INC and COMP.

MASK Data loaded into the MASK register operates on the data fed to the Mask Logic from the Counter Register. Loading new data into the MASK register automatically enables the Mask Logic. The Mask Logic is disabled either by loading zeros into the MASK register or by executing OP CODE <7> (Clear Counter Register/Mask disable). The Mask Logic will remain disabled until new data is loaded into the MASK register.
N.B. The MASK register can only be loaded from DI0-7.

START1 The START1 register can be loaded from either the DI0-7 inputs, or from the Counter Register. The contents of the START1 register may be forced into the Counter Register (OP CODE <6>), or may be used as a jump address in a conditional instruction.

START2 The START2 register can be loaded from either the DI0-7 inputs, or from the Counter Register. The contents of the START2 Register may be used as the jump address in a conditional instruction.

INC The INC register contains the value by which the counter will increment. This may be a positive or negative number, represented in 2's complement.
The INC register may be loaded either from the DI0-7 inputs, or from the Counter Register.

COMP The COMP register contains the value used by the comparator. It may be programmed from either the DI0-7 inputs or from the Counter Register.

8-Bit Adder

The 8-BIT ADDER adds the contents of the Inc and Counter Registers and loads the result into the Counter Register conditional on the current instruction.
The ADDER has a fast carry system which eliminates the need for external carry look-ahead circuitry when cascaded. Cascading is achieved by chaining CO to CI of the next most significant stage (see Fig.6).

Mask Logic

The MASK LOGIC is controlled by the contents of the Mask Register. 1's in the Mask Register will cause the corresponding outputs from the PDSP1640 to be frozen, even if the data in the Counter Register changes. In this manner 'windows' can be created within the counter's address field.
The MASK LOGIC is enabled whenever new data is loaded into the Mask Register. A zero word in the Mask Register will disable the MASK LOGIC as will executing OP CODE <7>.

Comparator

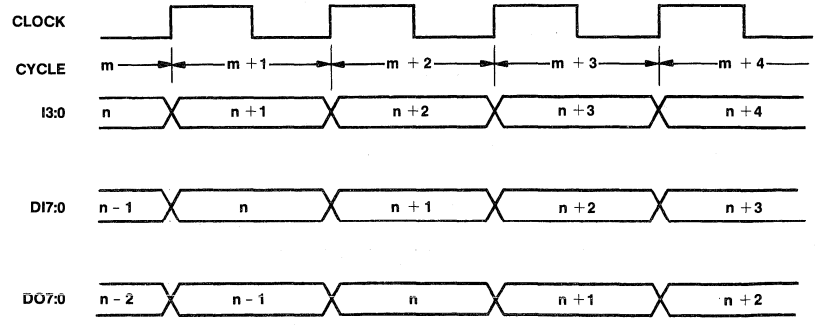
The COMPARATOR compares the value in the Comp Register with the output from the NEXT ADDRESS MUX. If the values are the same, then a signal is sent to the Control Decoder and onto the COMP output via the output register.

Control Decoder

The CONTROL DECODER has six inputs; the four instruction lines I0-3, CCEN, and an internal Comp Flag.
The CONTROL DECODER latches all except the CCEN input and the internal Comp Flag, on the rising edge of CLK. The I0-3 inputs are decoded to implement the operations shown in Table 2. CCEN and the Comp Flag change the instruction executed in the current cycle, where appropriate.

Next Address Mux and Counter Register

The contents of the COUNTER REGISTER at the start of a new cycle are determined by the NEXT ADDRESS MUX under the control of the Control Decoder.
The NEXT ADDRESS MUX selects between the DI0-7 inputs, the contents of START1 and 2, the contents of the Inc Register, and the output of the 8-bit Adder. The COUNTER REGISTER may be cleared by OP CODE <7>. The COUNTER REGISTER clock is inhibited for all instructions except those marked * in Table 2, this is to prevent the counter incrementing during register loads.



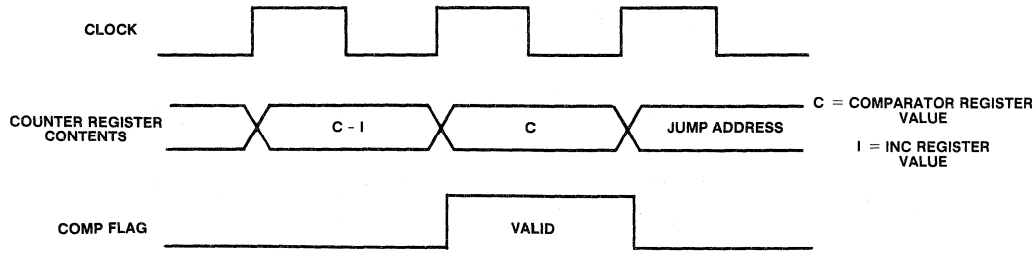
EXAMPLE
The result on DO7:0 on cycle m +3 is generated from data (DI7:0) applied on cycle m + 2 and the instruction (I3:0) applied on cycle m + 1.

Fig.4 Register delays

INSTRUCTION SET

Mnemonic	Op Code	Function
CCJDI	<0>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the data on DI0-7.
CCJS1	<1>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the contents of the Start1 Register.
CCJS2	<2>	On the next cycle the contents of the Counter Register will be added to the contents of the Increment Register and the result loaded into the Counter Register. If the COMP flag and CCEN become active, then on the following cycle, the Counter Register will be loaded with the contents of the Start2 Register.
LMRDI	<3>	Data present on DI0-7 will be loaded into the Mask Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRDI	<4>	The data present on DI0-7 will be loaded into the Counter Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRIR	<5>	The Counter Register will be loaded with the contents of the Inc Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
LCRS1	<6>	The Counter Register will be loaded with the contents of the Start1 Register by the rising edge of CLK at the end of the cycle in which this instruction is executed.
CLRCR	<7>	The Counter Register will be cleared and the Mask Logic disabled by the rising edge of CLK at the end of this instruction cycle.
LS1DI	<8>	The data present on DI0-7 will be loaded into the Start1 Register by the rising edge of CLK at the end of this instruction cycle.
LS1CR	<9>	The Start1 Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LS2DI	<A>	The data present on DI0-7 will be loaded into the Start2 Register by the rising edge of CLK at the end of this instruction cycle.
LS2CR	<B>	The Start2 Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LIRDI	<C>	The data present on the DI0-7 input will be loaded into the Inc Register by the rising edge of CLK at the end of this instruction cycle.
LIRCR	<D>	The Inc Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.
LCPDI	<E>	The data present on the DI0-7 inputs will be loaded into the Comp Register by the rising edge of CLK at the end of this instruction cycle.
LCPCR	<F>	The Comp Register will be loaded with the contents of the Counter Register by the rising edge of CLK at the end of this instruction cycle.

Table 1 Instruction descriptions



NOTE
A jump can also be forced by following LCPCR with CCJXX, provided the LCPCR instruction is held for two cycles prior to CCJXX.

Fig.5 Comparison flag timing

INSTRUCTION SET

Mnemonic	Code	I_3	I_2	I_1	I_0	Operation	Jump To
* CCJDI	0	0	0	0	0	Count by IR	DI0-7
* CCJS1	1	0	0	0	1	Count by IR	START1
* CCJS2	2	0	0	1	0	Count by IR	START2
LMRDI	3	0	0	1	1	Ld MR from DI0-7	
* LCRDI	4	0	1	0	0	Ld CR from DI0-7	
* LCRIR	5	0	1	0	1	Ld CR from IR	
* LCRS1	6	0	1	1	0	Ld CR from S1	
CLRCR	7	0	1	1	1	Clear CR/MR	
LS1DI	8	1	0	0	0	Ld S1 from DI0-7	
LS1CR	9	1	0	0	1	Ld S1 from CR	
LS2DI	A	1	0	1	0	Ld S2 from DI0-7	
LS2CR	B	1	0	1	1	Ld S2 from CR	
LIRDI	C	1	1	0	0	Ld IR from DI0-7	
LIRCR	D	1	1	0	1	Ld IR from CR	
LCPDI	E	1	1	1	0	Ld CP from DI0-7	
LCPCR	F	1	1	1	1	Ld CP from CR	

All instructions executed on the next rising edge of CLK. * indicates instructions which do not inhibit the counter register clock.

Table 2 Instruction set codes

Key

IR = Increment Register
MR = Mask Register
CR = Counter Register
S1 = Start1 Register
S2 = Start2 Register
CP = Comparator Register

Mnemonics

CCJXX = Conditional Count, Jump to XX
LXXYY = Load Destination XX from Source YY
CLRCR = Clear Counter Register/Reset Mask Logic

COUNTER CONFIGURATIONS

Fig.6 illustrates chaining of PDSP1640s to 16 bits and Fig.7 the configuration for a 24-bit address generator. The cascaded devices have exactly the same functions as a single device.

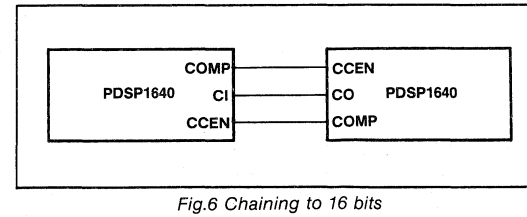


Fig.6 Chaining to 16 bits

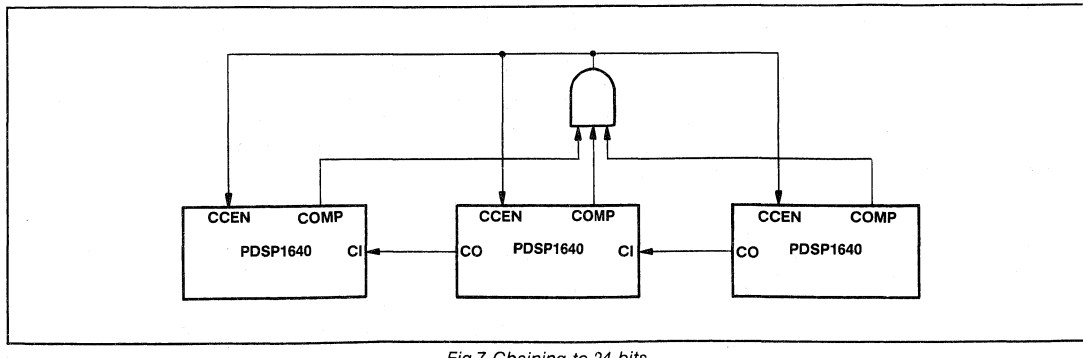


Fig.7 Chaining to 24 bits

TYPICAL APPLICATION

In the application shown in Fig.8 two PDSP1640s are used as an address generator in a digital waveform generator capable of producing complex waveforms at very high speeds. The programmable registers in the PDSP1640 allow the host microprocessor to control both frequency (by altering Step Size) and waveshape (by selecting different wavetables by Start Address).

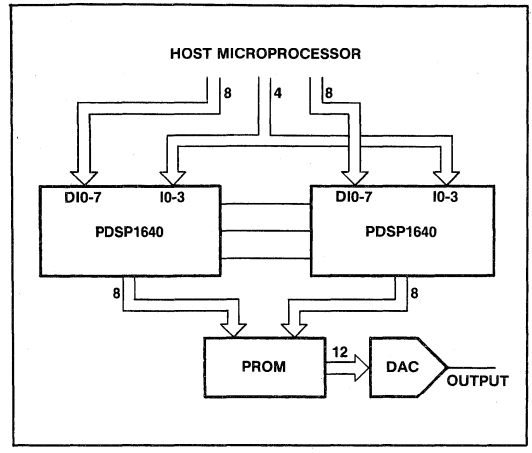


Fig.8 Arbitrary waveform generation

TYPICAL APPLICATION

Mnemonic	Op Code	Operation	Data
CLRCR	<7>	Clear CR/MR	X
LCRDI	<4>	Load CR	X
LIRDI	<C>	Load Inc Register	Start addr
LS1DI	<8>	Ld SR1 with branch addr	Step size
LCPDI	<E>	Ld COMPR with stop addr	Branch addr
CCJS1	<1>	Count by INC/goto SR1	Stop addr

Table 3 Typical instruction sequence for Fig.8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V
T_{amb} (Commercial) = 0°C to +70°C, V_{CC} = 5.0V ± 5%, GND = 0V
T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	I_{OH} = 8mA
Output low voltage	V_{OL}			0.6	V	I_{OL} = -8mA
Input high voltage	V_{IH}	2.2			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}	-10		10	μA	GND ≤Vin≤Vcc
Output leakage current	I_{OZ}	-50		50	μA	GND ≤V_{OUT}≤Vcc = Vcc max.
Output short cct current (Note 2)	I_{OS}	40		250	mA	Vcc = max.
Input capacitance	C_{IN}		9		pF	LC and HC packages
			12		pF	DG and DP packages

Switching Characteristics

Characteristic	Value								Units	Conditions
	Industrial			Commercial			Military			
	PDSP1640 B0			PDSP1640A C0			PDSP1640 A0			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Max.		
CKL frequency			20		45			20	MHz	
CLK high period	20			12	6		20		ns	
CLK low period	15			10	8		15		ns	
CLK to CO			44		25	34		44	ns	1 LSTTL +5pF load
CLK to DO			34		21	27		34	ns	2 LSTTL +20pF load Opcode 3
CLK to DO			28		19	22		28	ns	2 LSTTL +20pF load Remaining Opcodes
CLK to COMP			35		19	30		35	ns	50pF load (Opcode 0,1,2)
CI to CO			20		12	16		20	ns	1 LSTTL +5pF load
Setup DI to CLK	10			10	5		10		ns	
Hold DI to CLK	3			3	0		3		ns	
Setup CI to CLK	20			15	8		20		ns	
Hold CI to CLK	3			3	0		3		ns	
Setup I to CLK	15			10	5		15		ns	
Hold I to CLK	3			3	0		3		ns	
Setup CCEN to CLK	30			18	15		30		ns	
Hold CCEN to CLK	0			0	0		0		ns	
$\overline{OE}$ high to DO High Z			30			20		30	ns	See $\overline{OE}$ test diagrams Fig.9
$\overline{OE}$ low to DO/COMP valid			22			16		22	ns	
V_{CC} current			20			40		20	mA	V_{CC} = Max. outputs unloaded CLK Freq = Max.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5 to 7.0V
Input voltage V_{IN}	-0.9 to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9 to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	±18mA
Static discharge voltage (HMB)	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Military	-55°C to +125°C
Industrial	-40°C to +85°C
Commercial	0°C to +70°C
Junction temperature	150°C
Package power dissipation	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
DG	12	40
LC	13	56
HC	13	56

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H — 0.5V
Delay from output low to output high impedance	V_L — 0.5V
Delay from output high impedance to output low	1.5V — 0.5V
Delay from output high impedance to output high	1.5V — 0.5V

NOTES
1. V_H - Voltage reached when output driven high.
2. V_L - Voltage reached when output driven low.

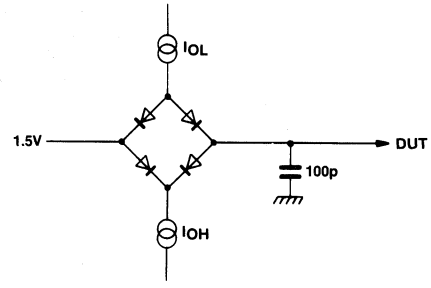


Fig.9 Three state delay measurement load

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP1640 B0 DG (Ceramic DIL package)
PDSP1640 B0 DP (Plastic DIL package)
PDSP1640 B0 LC (Leadless chip carrier)
PDSP1640 B0 HC (Leaded chip carrier)

Military (-55°C to +125°C)

PDSP1640 A0 DG (Ceramic DIL package)
PDSP1640 A0 LC (Leadless chip carrier)
PDSP1640 A0 HC (Leaded chip carrier)

Commercial (0°C to +70°C)

PDSP1640A C0 DG (Ceramic DIL package)
PDSP1640A C0 DP (Plastic DIL package)
PDSP1640A C0 LC (Leadless chip carrier)
PDSP1640A C0 HC (Leaded chip carrier)

PLESSEY
Semiconductors

PDSP16112/PDSP16112A

16 x 12 BIT COMPLEX MULTIPLIER

(SUPERSEDES MARCH 1987 EDITION)

The PDSP16112/PDSP16112A will multiply a complex (16 + 16) bit data word by a complex (12 + 12) bit coefficient word and produce a complex (17 + 17) bit rounded product. The input data format is two's complement. The device consists of four 16 x 12 multiplier sections based on Booth's '2 bits at a time' algorithm and is pipelined to achieve a 20MHz (PDSP16112A) or 10MHz (PDSP16112) throughput.

FEATURES

- 20MHz Complex Number (16 + 16) x (12 + 12) Multiplication
- Pipelined Architecture
- Power Dissipation only 500mW
- TTL Compatible Inputs
- Advanced 2 micron CMOS Process

APPLICATIONS

- Digital Filtering
- Fast Fourier Transforms
- Radar and Sonar Processing
- Instrumentation
- Automation
- Image Processing

ASSOCIATED PRODUCTS

PDSP1601 Arithmetic Logic Unit
PDSP1640 40MHz Address Generator
PDSP16318 Complex Accumulator
PDSP16330 Pythagoras Processor

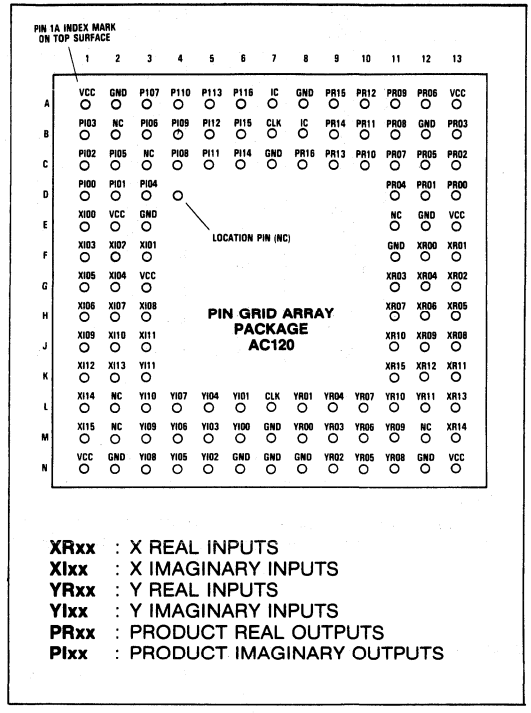


Fig.1 Pin connections - top view

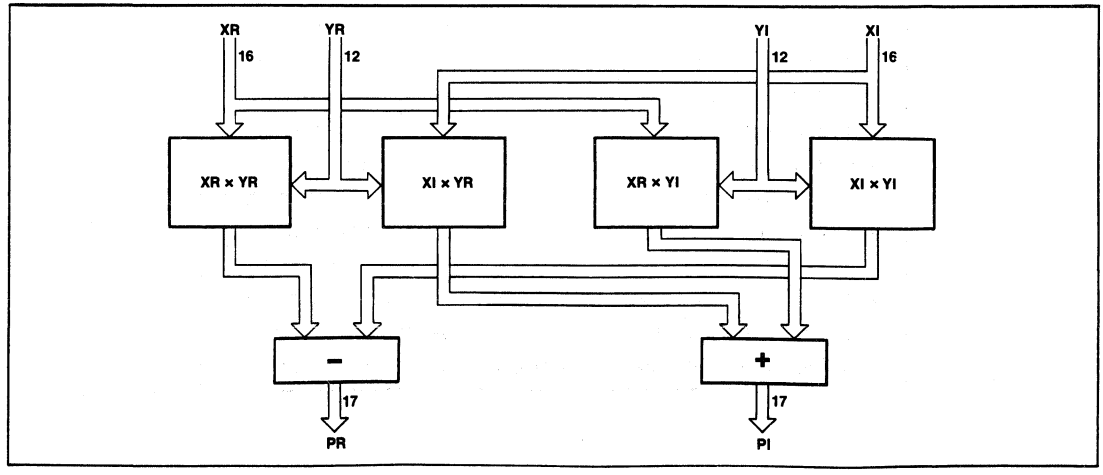


Fig.2 Multiplier block diagram

PIN OUT - FUNCTION TO PIN

Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.
PR00	D13	PR09	A11	PI00	D1	PI09	B4
PR01	D12	PR10	C10	PI01	D2	PI10	A4
PR02	C13	PR11	B10	PI02	C1	PI11	C5
PR03	B13	PR12	A10	PI03	B1	PI12	B5
PR04	D11	PR13	C9	PI04	D3	PI13	A5
PR05	C12	PR14	B9	PI05	C2	PI14	C6
PR06	A12	PR15	A9	PI06	B3	PI15	B6
PR07	C11	PR16	C8	PI07	A3	PI16	A6
PR08	B11	CLK	L7	PI08	C4	CLK	B7
XR00	F12	XI00	E1	YR00	M8	YI00	M6
XR01	F13	XI01	F3	YR01	L8	YI01	L6
XR02	G13	XI02	F2	YR02	N9	YI02	N5
XR03	G11	XI03	F1	YR03	M9	YI03	M5
XR04	G12	XI04	G2	YR04	L9	YI04	L5
XR05	H13	XI05	G1	YR05	N10	YI05	N4
XR06	H12	XI06	H1	YR06	M10	YI06	M4
XR07	H11	XI07	H2	YR07	L10	YI07	L4
XR08	J13	XI08	H3	YR08	N11	YI08	N3
XR09	J12	XI09	J1	YR09	M11	YI09	M3
XR10	J11	XI10	J2	YR10	L11	YI10	L3
XR11	K13	XI11	J3	YR11	L12	YI11	K3
XR12	K12	XI12	K1	NC	B2	NC	M12
XR13	L13	XI13	K2	NC	L2	NC	M2
XR14	M13	XI14	L1	VCC	A1	NC	E11
XR15	K11	XI15	M1	VCC	G3	NC	C3
GND	N12	GND	C7	VCC	E2	GND	N8
GND	N7	GND	A2	VCC	A13	GND	N6
GND	M7	GND	E12	VCC	E13	GND	F11
GND	N2	GND	E3	VCC	N1	IC	B8
GND	A8	GND	B12	VCC	N13	IC	A7

NOTE
IC = Internally connected - do not connect to these pins.
All inputs are internally connected to V_{CC} by 10k (nominal) resistors.

PIN OUT - PIN TO FUNCTION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VCC	GND	PI07	PI10	PI13	PI16	IC	GND	PR15	PR12	PR09	PR06	VCC
B	PI03	NC	PI06	PI09	PI12	PI15	CLK	IC	PR14	PR11	PR08	GND	PR03
C	PI02	PI05	NC	PI08	PI11	PI14	GND	PR16	PR13	PR10	PR07	PR05	PR02
D	PI00	PI01	PI04								PR04	PR01	PR00
E	XI00	VCC	GND								NC	GND	VCC
F	XI03	XI02	XI01								GND	XR00	XR01
G	XI05	XI04	VCC								XR03	XR04	XR02
H	XI06	XI07	XI08								XR07	XR06	XR05
J	XI09	XI10	XI11								XR10	XR09	XR08
K	XI12	XI13	YI11								XR15	XR12	XR11
L	XI14	NC	YI10	YI07	YI04	YI01	CLK	YR01	YR04	YR07	YR10	YR11	XR13
M	XI15	NC	YI09	YI06	YI03	YI00	GND	YR00	YR03	YR06	YR09	NC	XR14
N	VCC	GND	YI08	YI05	YI02	GND	GND	GND	YR02	YR05	YR08	GND	VCC

PIN DESCRIPTION

XR00 - XR15	X Real Inputs : Two's Complement Format XR15 = MSB (Sign) XR00 = LSB For Fractional Arithmetic the Weighting of XR15 = 1 i.e. -1≤ XR<1	PR00 - PR16	P Real Outputs : Two's Complement Format PR16 = MSB (Sign) PR00 = LSB For Fractional Arithmetic the Weighting of PR16 = 2 i.e. -2≤ PR<2
XI00 - XI15	X Imag Inputs : Two's Complement Format XI15 = MSB (Sign) XI00 = LSB For Fractional Arithmetic the Weighting of XI15 = 1 i.e. -1≤ XI<1	PI00 - PI16	P Imag Outputs : Two's Complement Format PI16 = MSB (Sign) PI00 = LSB For Fractional Arithmetic the Weighting of PI16 = 2 i.e. -2≤ PI<2
YR00 - YR11	Y Real Inputs : Two's Complement Format YR11 = MSB (Sign) YR00 = LSB For Fractional Arithmetic the Weighting of YR11 = 1 i.e. -1≤ YR<1	CLK pin B7 and pin L7	Common Clock to all on chip registers, both pins must be connected
		VCC GND	All VCC and GND pins must be connected
YI00 - YI11	Y Imag Inputs : Two's Complement Format YI11 = MSB (Sign) YI00 = LSB For Fractional Arithmetic the Weighting of YI11 = 1 i.e. -≤ YI<1	IC	Internally connected - do not use

FUNCTIONAL DESCRIPTION

The PDSP16112 Complex Multiplier contains four pipelined 16x12 Array Multipliers, a 17-bit adder and a 17-bit subtractor.

The multipliers accept data from the XR, XI, YR, and YI inputs and perform the four multiplies necessary to implement a Complex Multiply Operation,

(XR x YR, XR x YI, XI x YR, XI x YI).

The 28-bit results from these operations are rounded to the most significant 16-bits before being passed to the adder and subtractor. The subtractor calculates

(XR x YR) - (XI x YI)

to form a 17-bit result representing the real result of the complex multiplication. The adder calculates

(XR x YI) + (XI x YR)

to form a 17-bit result that represents the imaginary result of the complex multiplication. These real and imaginary results are passed to the PR and PI outputs respectively.

The add and subtract operations may, (depending upon the data), cause the multiplier results to grow by one bit hence requiring 17-bit outputs to represent the results. The PDSP16112 is designed to operate with two's complement arithmetic, hence if the Fractional two's complement format is used the outputs will lie in the range

$-2 \leq P < 2$

for inputs in the range

$-1 \leq X \text{ or } Y < 1.$

If the output magnitude lies in the range

$-1 \leq P < 1,$

then the 17th (MSB) bit of the outputs will duplicate the 16th (Sign) bit of the output.

In common with other Array multipliers, the operation

-1 x -1

will yield an incorrect result for fractional two's complement formats, and hence should be avoided.

Both X and Y inputs are registered as are the PR and PI outputs. On the rising edge of CLK data present on the XR, XI, YR, and YI inputs is clocked into the input registers. At the same time a new result is clocked into the output registers and made available on the PR and PI output ports.

Pipelined Operation

The internal Multiply and Add operations are divided into stages by six internal pipeline registers giving a total latency through the device of eight clock cycles. This means that the result from data loaded into the device on the first clock cycle appears at the outputs during the seventh clock cycle, and may be loaded into another device on the eighth clock cycle.

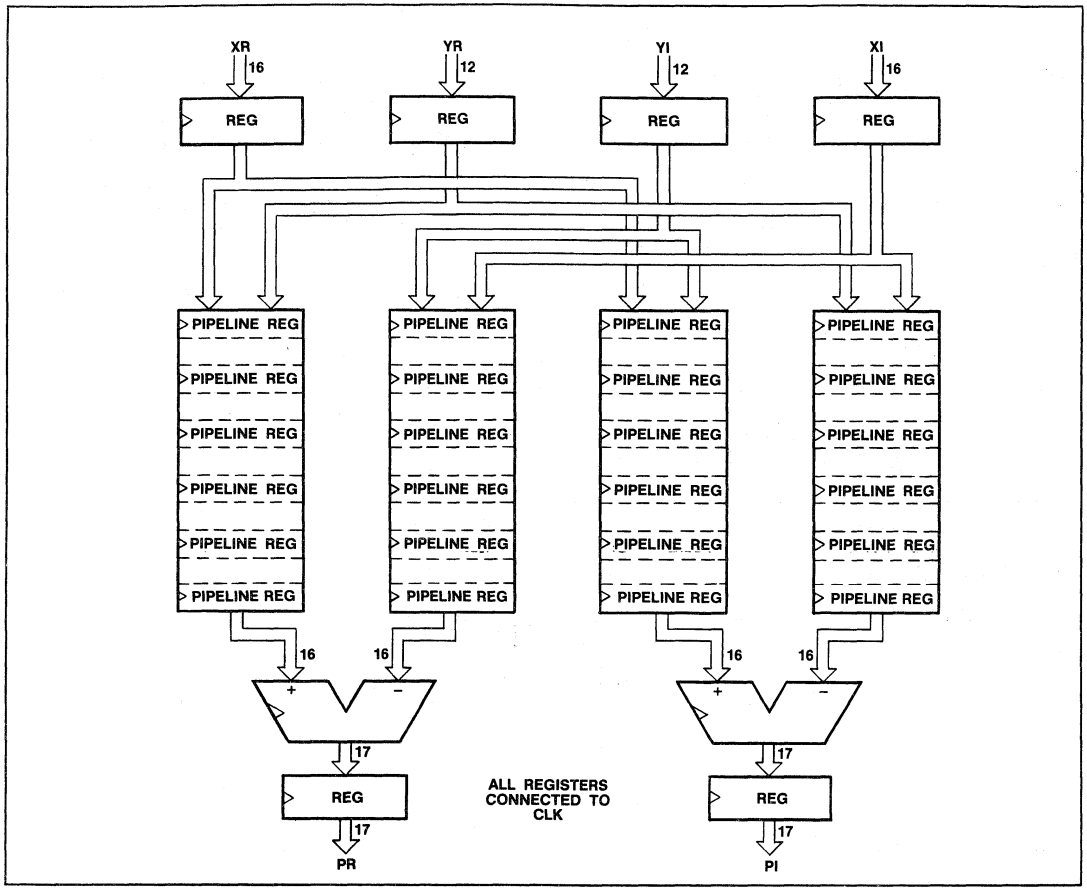


Fig.3 Pipelined multiplier structure

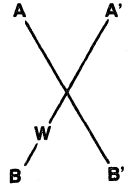
TYPICAL APPLICATION

The PDSP16112A may be configured as the main arithmetic element in a FFT Butterfly calculation. A single PDSP16112A together with two PDSP16318As will produce an arithmetic processor capable of executing a new Radix 2 DIT Butterfly every 50ns using 16-bit data and 12-bit coefficients. The PDSP16318A provides flags that monitor the magnitude of the output data, together with on chip shift circuits.

A single Butterfly processor of this type will allow the following FFT benchmarks.

1024 point complex radix 2 transform in 256μsecs
512 point complex radix 2 transform in 115μsecs
256 point complex radix 2 transform in 51μsecs

The arithmetic operation required to realise a radix 2 decimation in time algorithm is as follows.



$$A' = A + (B \times W)$$

$$B' = A - (B \times W)$$

Where A and B are the data inputs, A' and B' are the data outputs, and W is the coefficient. A,B,A',B' and W are all complex numbers i.e. they all have real and imaginary components. The Butterfly therefore requires one complex multiply and two complex adds to execute, which is equivalent to four real multiplies and six real adds.

Fig.4 illustrates the interconnection of the PDSP16112 with the two PDSP16318A Complex Accumulators. The PDSP16112 performs the complex multiply operation at the full 20MHz rate to provide the real and imaginary components of (B x W) to the two ALUs. The PDSP16318A is capable of 16-bit operations at 20MHz and has on chip register storage and Shifter. In every 20MHz cycle each PDSP16318A performs two arithmetic operations to calculate the real or imaginary parts of A + (B x W) and A - (B x W). One of the PDSP16318As calculates the real parts and the other calculates the imaginary parts.

For greater throughput one chip-set may be allocated to each column of the FFT. For example, a 1K complex FFT could be calculated by 10 chip-sets every 26μs.

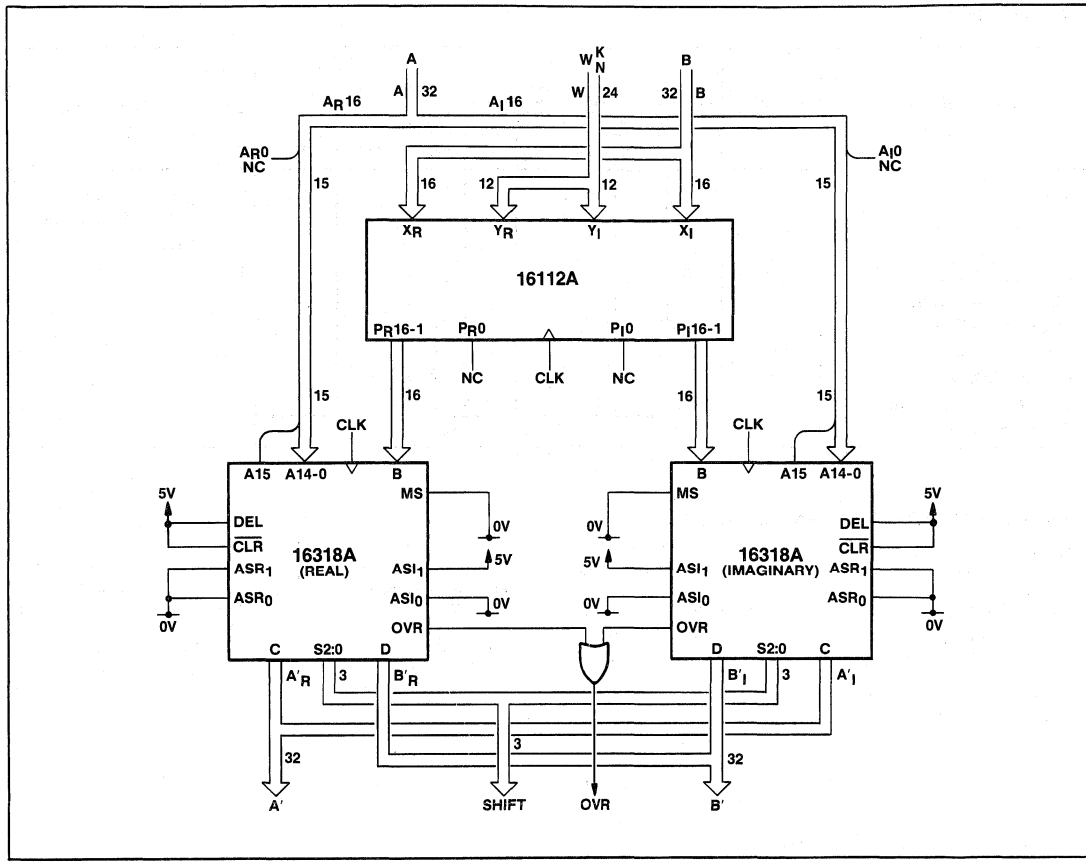


Fig.4 Radix 2 DIT butterfly processor

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value						Units	Conditions
		PDSP16112			PDSP16112A				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			2.4			V	I_{OH} = 4mA
Output low voltage	V_{OL}			0.6			0.6	V	I_{OL} = 4mA
Input high voltage	V_{IH}	2.2			2.2			V	
Input low voltage	V_{IL}			0.8			0.8	V	
Input leakage current *	I_L	-1.0		+0.01	-1.0		+0.01	mA	$GND \leqslant V_{IN} \leqslant V_{CC}$
Output short circuit current	I_{OS}	15			20			mA	V_{CC} = max.
Input capacitance	C_I		10			10		pF	

*All inputs have a nominal 10K pull-up resistor to V_{CC}.

AC Characteristics

Characteristic	Symbol	Value Industrial						Value Military		Units	Conditions
		PDSP16112			PDSP16112A						
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{CC} current	I_{CC}			90			170		90	mA	V_{CC} = max Outputs unloaded f_{CLK} = max
Max. CLK frequency	f_{CLK}	10			20			10		MHz	
Min. CLK frequency				DC			DC		DC		
Input setup time	t_{su}			30			20		30	ns	
Input hold time	t_{ih}			5			5		5	ns	
CLK to output delay	t_d			50			30		50	ns	
CLK Mark/Space ratio		40		60	40		60	40	60	%	
Drive capability		2 x LSTTL +20pF									

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	±18mA
Static discharge voltage	500V
Storage temperature range T_S	-65°C to +150°C
Junction temperature	150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Package power dissipation P_{TOT}	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
AC	11	35

ORDERING INFORMATION

Industrial
PDSP16112 B0 AC
PDSP16112A B0 AC

Military
PDSP16112 A0 AC

Call for availability of Hi-Rel parts and MIL-883C screening.

PDSP16116

16 BY 16 BIT COMPLEX MULTIPLIER

The PDSP16116 will multiply two complex (16 + 16) bit words every 100ns and can be configured to output the complete complex (32 + 32) bit result within a single cycle. The data format is fractional two's complement.

The PDSP16116 contains four 16 x 16 Array Multipliers, two 32 bit Adder/Subtractors and all the control logic required to support Block Floating Point Arithmetic as used in FFT applications. In combination with a PDSP16318, the PDSP16116 forms a two chip 10MHz Complex Multiplier-Accumulator with 20 bit accumulator registers and output shifters. The PDSP16116 in combination with two PDSP16318s and two PDSP1601's forms a complete 10MHz Radix 2 DIT FFT Butterfly solution which fully supports Block Floating Point Arithmetic. The PDSP16116 has an extremely high throughput that is suited to recursive algorithms as all calculations are performed with a single pipeline delay (two cycle fall-through).

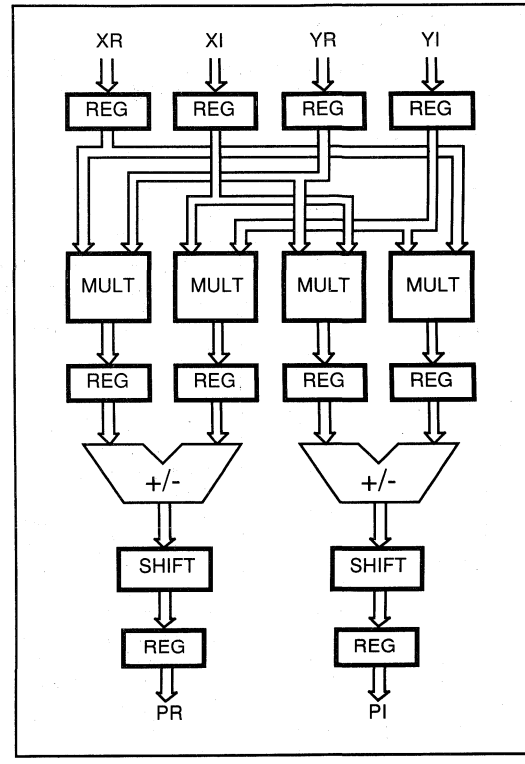


Fig. 1 Simplified Block Diagram

FEATURES

- Complex Number (16 + 16) X (16 + 16) Multiplication
- Full 32 bit Result
- 10MHz Clock Rate
- Block Floating Point FFT Butterfly Support
- -1 times -1 Trap
- Two's Complement Fractional Arithmetic
- TTL Compatible I/O
- Complex Conjugation
- 2 Cycle Fall Through

APPLICATIONS

- Fast Fourier Transforms
- Digital Filtering
- Radar and Sonar Processing
- Instrumentation
- Image Processing

ASSOCIATED PRODUCTS

PDSP16318/A	Complex Accumulator
PDSP16112/A	(16 + 16) x (12 + 12) Complex Multiplier
PDSP16330	Pythagoras Processor
PDSP1601/A	Augmented Arithmetic Logic Unit
PDSP1640/A	40MHz Address Generator

The PDSP16116 has a number of features tailored for System applications:

-1 x -1 Trap

In multiply operations utilising Twos Complement Fractional notation, the -1 x -1 operation forms an invalid result as +1 is not representable in the fractional number range. The PDSP16116 eliminates this problem by trapping the -1 x -1 operation and forcing the Multiplier result to become the most positive representable number.

Complex Conjugation

Many algorithms utilising complex arithmetic require conjugation of complex data streams. This operation has traditionally required an additional ALU to multiply the imaginary component by -1. The PDSP16116 eliminates the requirement for the extra ALU by offering on chip complex conjugation of either of the two incoming complex data words with no loss in throughput.

Easy Interfacing

As with all PDSP family members the PDSP16116 has registered I/O for data and control. Data inputs have independent clock enables and data outputs have independent three state output enables.

Signal	Type	Description	Normal mode Configuration
XR15:0	INPUT	16 bit input for real x data	
XI15:0	INPUT	16 bit input for imag x data	
YR15:0	INPUT	16 bit input for real y data	
YI15:0	INPUT	16 bit input for imag y data	
PR15:0	OUTPUT	16 bit output for real p data	
PI15:0	OUTPUT	16 bit output for imag p data	
CLK	INPUT	Clock, new data is loaded on rising edge of CLK	
$\overline{CEX}$	INPUT	Clock enable X-port input register	
$\overline{CEY}$	INPUT	Clock enable Y-port input register	
CONX	INPUT	Conjugate X data	
CONY	INPUT	Conjugate Y data	
ROUND	INPUT	Rounds the real & imag results	
MBFP	INPUT	Mode select (BFP/Normal)	Tie Low
$\overline{SOBFP}$	INPUT	Start of BFP operations **	Tie Low
$\overline{EOPSS}$	INPUT	End of pass **	Tie Low
AR15:13	INPUT	3 MSB's from real part of A-word **	Tie Low
AI15:13	INPUT	3 MSB'S from imag part of A-word **	Tie Low
WTA1:0	INPUT	Word tag from A-word **	Tie Low
WTB1:0	INPUT	Word tag from B-word / shift control *	
WTOUT1:0	OUTPUT	Word tag output**	
SFTA1:0	OUTPUT	Shift control for A-word / overflow flag *	
SFTR2:0	OUTPUT	Shift control for accumulator result **	
GWR4:0	OUTPUT	Global weighting register contents **	
$\overline{OSEL1:0}$	INPUT	Selects the desired output configuration	
$\overline{OER}$, $\overline{OEI}$	INPUT	Output enables	
VDD	POWER	+5V Supply All supply pins	
GND	POWER	0V Supply must be connected	

* Indicates pin performs different functions in BFP / Normal modes.
** Indicates pin is used only in BFP mode

Table 1 Signal Descriptions

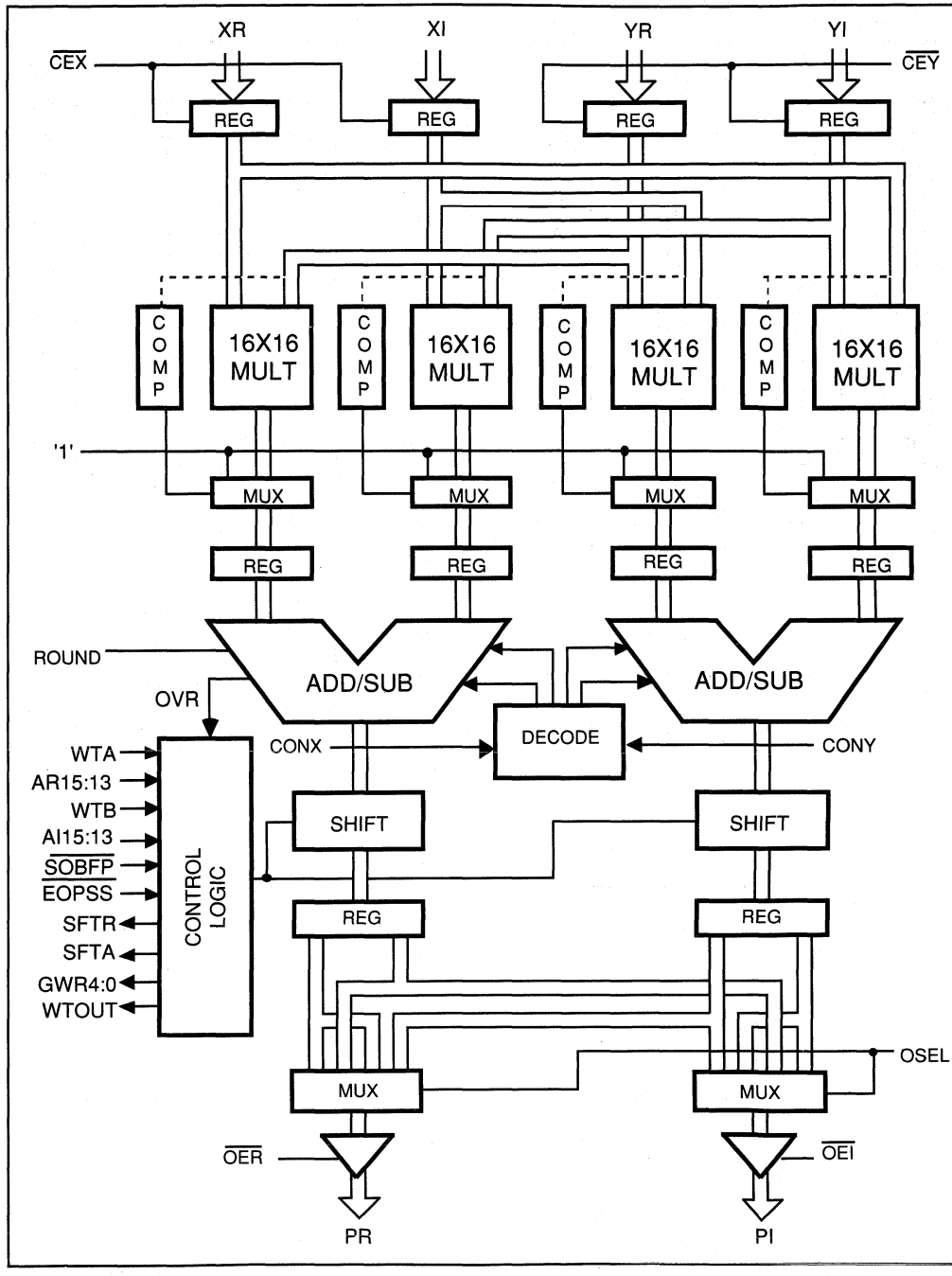


Fig. 2 Block Diagram

Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No
AI13	G2	PI8	B4	VDD	C6	XR12	R10
AI14	G3	PI9	C5	VDD	A1	XR13	R9
AI15	F1	PI10	B3	WTA0	G14	XR14	N9
AR13	G1	PI11	A2	WTA1	F15	XR15	N8
AR14	H2	PI12	C4	WTB0	G15	YI0	M3
AR15	H1	PI13	C3	WTB1	G13	YI1	P1
$\overline{\text{CEX}}$	R8	PI14	D3	WTOUT0	D2	YI2	N2
$\overline{\text{CEY}}$	P8	PI15	C2	WTOUT1	B1	YI3	L3
CLK	F13	PR0	C8	XI0	N3	YI4	M2
CONX	F3	PR1	A8	XI1	N4	YI5	N1
$\overline{\text{CONY}}$	F2	PR2	B8	XI2	P3	YI6	M1
$\overline{\text{EOPSS}}$	H14	PR3	A9	XI3	R2	YI7	L2
GND	P2	PR4	A10	XI4	P4	YI8	L1
GND	M13	PR5	A11	XI5	N5	YI9	K3
GND	B13	PR6	B10	XI6	R3	YI10	K2
GND	B9	PR7	C10	XI7	P5	YI11	J2
GND	B5	PR8	A12	XI8	R4	YI12	K1
GND	B2	PR9	B11	XI9	N6	YI13	J1
GWR0	E13	PR10	A13	XI10	P6	YI14	J3
GWR1	C14	PR11	C11	XI11	R5	YI15	H3
GWR2	B15	PR12	B12	XI12	P7	YR0	J15
GWR3	D13	PR13	A14	XI13	N7	YR1	K15
GWR4	C13	PR14	A15	XI14	R6	YR2	J13
$\overline{\text{MBFP}}$	F14	PR15	B14	XI15	R7	YR3	J14
$\overline{\text{OER}}$	D15	ROUND	E1	XR0	N12	YR4	L15
$\overline{\text{OEI}}$	D1	SFTA0	C15	XR1	R14	YR5	K14
OSEL0	E14	SFTA1	D14	XR2	P13	YR6	K13
OSEL1	E15	SFTR0	E3	XR3	N11	YR7	M15
PI0	C7	SFTR1	C1	XR4	P12	YR8	L14
PI1	A7	$\overline{\text{SFTR2}}$	E2	XR5	R13	YR9	N15
PI2	A6	$\overline{\text{SOBFP}}$	H13	XR6	R12	YR10	L13
PI3	B7	VDD	R1	XR7	P11	YR11	M14
PI4	B6	VDD	N14	XR8	R11	YR12	P15
PI5	A5	VDD	C12	XR9	N10	YR13	R15
PI6	A4	VDD	C9	XR10	P10	YR14	P14
PI7	A3	VDD	H15	XR11	P9	YR15	N13

Table 2 Pin Allocations

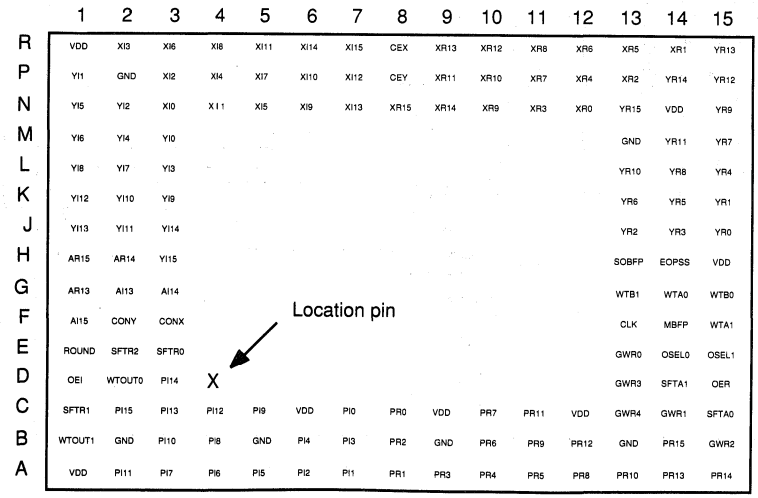


Fig. 3 Pin Allocation Diagram (Bottom view)

NORMAL MODE OPERATION

When the MBFP mode select input is held low the 'Normal' mode of operation is selected. This mode supports all Complex Multiply operations that do not require Block Floating Point arithmetic.

Multiplier Stage

Complex twos complement fractional data is loaded into the X and Y input registers via the X and Y Ports on the rising edge of CLK. The Real and Imaginary components of the fractional data are each assumed to have the following format.

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Where S = sign bit which has an effective weighting -2^0

The value of the 16 bit two's complement word is

Value = $(-1xS)+(bit14x2^{-1})+(bit13x2^{-2})+(bit12x2^{-3})$ . . .

The X & Y port registers are individually enabled by the $\overline{CEX}$ & $\overline{CEY}$ signals respectively. If the registers are required to be permanently enabled, then these signals may be tied to ground. On each clock cycle the contents of the input registers are passed to the four multipliers to start a new Complex Multiply operation. Each Complex Multiply operation requires four partial products (Xr x Yr), (Xr x Yi), (Xi x Yr), (Xi x Yi), all of which are calculated in parallel by the four 16x16 Multipliers. Only one clock cycle is required to complete the multiply stage before the Multiplier results are loaded into the Multiplier output registers for passing on to the Adder/Subtractors in the next cycle. Each multiplier produces a 31bit result with the duplicate sign bit eliminated. The format of the output data from the Multipliers is

BIT NUMBER	30	29	28	27	26	25	24	···	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	····	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^0

Result Correction

Due to the nature of fractional twos complement representation it is possible to represent -1 exactly but not 1. With conventional multipliers this causes a problem when -1 is multiplied by -1 as the multiplier produces an incorrect result. The PDSP16116 includes a trap to ensure that the most positive number (value = $1 - 2^{-30}$), (hex =7FFFFFFF) is substituted for the incorrect result. The multiplier result is therefore always a (correct) fractional value.

Complex Conjugation

Either the X or Y input data may be complex conjugated by asserting the CONX or CONY signals respectively. Asserting either of these signals has the effect of inverting (multiplying by -1) the imaginary component of the respective input. Table 3 shows the effect of CONX and CONY on the X and Y inputs.

FUNCTION	OPERATION	CONX	CONY
X x Y	(XR+XI)x(YR+YI)	low	low
X x Conj Y	(XR+XI)x(YR-YI)	low	high
Conj X x Y	(XR-XI)x(YR+YI)	high	low
Invalid	Invalid	high	high

Table 3 Conjugate Functions

Adder / Subtractor Stage

The 31bit Real and Imaginary results from the Multipliers are passed to two 32 bit Adder / Subtractors. The Adder calculates the imaginary result ((Xr x Yi) + (Xi x Yr)) and the Subtractor calculates the Real result ((Xr x Yr) - (Xi x Yi)). Each Adder / Subtractor produces a 32 bit result with the following format.

BIT NUMBER	31	30	29	28	27	26	···	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	·····	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^1

Rounding

The ROUND control when asserted rounds the most significant 16 bits of the full 32 bit result from the Adder/ subtractor. If the ROUND signal is active (High), then bit 16 is set to a one, rounding the most significant 16 bits of the Adder/ Subtractor result. (The least significant 16 bits are unaffected). Inserting a one ensures that the rounding error is never greater than 1LSB, and that no DC bias is introduced as a result of the rounding process.

The format of the Rounded result is;

BIT NUMBER	31	30	29	28	27	·····	18	17	16	15	14	13	·····	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	·····	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	·····	2^{-28}	2^{-29}	2^{-30}
	← ROUNDED VALUE →													← LBS's →		

The effective weighting of the sign bit is -2^1

Shifter

Each of the two Adder / Subtractors are followed by Shifters controlled via the WTB control input. These shifters can each apply four different shifts, however the same shift is applied to both real and imaginary components. The four shift options are:

i) WTB1:0 = 11 Shift complex product one place to the left giving a shifter output format:

BIT NUMBER	31	30	29	28	27	26	25	···	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	····	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

The effective weighting of the sign bit is -2^0.

ii) WTB1:0 = 00 No shift applied giving a shifter output format:

BIT NUMBER	31	30	29	28	27	26	···	8	7	6	5	4	3	2	1	0
WEIGHTING	S	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	·····	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

The effective weighting of the sign bit is -2^{1}.

iii) WTB1:0 = 01 Shift complex product one place to the right giving a shifter output format:

BIT NUMBER	31	30	29	28	27	26	25	24	···	6	5	4	3	2	1	0
WEIGHTING	S	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	···	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}

The effective weighting of the sign bit is -2^{2}.

iv) WTB1:0 = 10 Shift complex product two places to the right giving a shifter output format:

BIT NUMBER	31	30	29	28	27	26	25	24	···	6	5	4	3	2	1	0
WEIGHTING	S	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	···	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}

The effective weighting of the sign bit is -2^{3}.

Overflow

If the left shift option is selected and the Adder / Subtractors contain a 32 bit word, then an invalid result will be passed to the output. An invalid output arising from this combination of events will be flagged by the SFTA0 flag output. The SFTA0 Flag will go high if either the real or imaginary result is invalid.

Output Select

The output from the Shifters is passed to the Output Select Mux, which is controlled via the OSEL inputs. These inputs are not registered and hence allow the output combination to be changed within each cycle. The full complex 64 bit result from the multiplier may therefore be output within a single cycle. The OSEL control selects four different output combinations as summarised in Table 4.

OSEL1	OSEL0	PR	PI
0	0	MSR	MSI
0	1	LSR	LSI
1	0	MSR	LSR
1	1	MSI	LSI

Table 4 Output Selection

(Where MSR and LSR are the most and least significant 16 bit words of the Real Shifter output, MSI and LSI are the most and least significant 16 bit words of the Imaginary Shifter output).

The output select options allow two different modes for extracting the full 32 bit result from the PDSP16116. The first mode treats the two 16 bit outputs as real and imaginary ports allowing the real and imaginary results to be output in two halves on the real and imaginary output ports. The second mode treats the two 16 bit outputs as one 32 bit output and allows the real and imaginary results to be output as 32 bit words.

PIN DESCRIPTION

XR, XI, YR, YI

Data inputs 16 bits: Data is loaded into the input registers from these ports on the rising edge of CLK. The data format is Twos Complement Fractional, where the MSB (sign bit) is bit 15. In normal mode the weighting of the MSB is -2^{0} ie -1.

PR, PI

Data outputs 16 bits: Data is clocked into the output registers and passed to the PR and PI outputs on the rising edge of CLK. The data format is Twos Complement Fractional. The field of the internal result selected for output via PR and PI is controlled by signals OSEL1:0 (see Table 4).

CLK

Common Clock to all internal registers.

$\overline{\text{CEX}}$, $\overline{\text{CEY}}$

Clock enables for X and Y input ports: When low these inputs enable the CLK signal to the X or Y input registers allowing new data to be clocked into the Multiplier.

CONX, CONY

If either of these inputs are high on the rising edge of CLK, then the data in the associated input has its imaginary component inverted (multiplied by -1), see Table 3. CONX and CONY affect data input on the same clock rising edge.

ROUND

The ROUND control is used to round the most significant 16 bits of the Adder/Subtractor result prior to being passed to the output registers. The rounding operation takes place one cycle after the ROUND input is taken high providing rounded outputs on the second cycle after ROUND is taken high. The ROUND input is not latched and is intended to be tied high or low depending upon the application.

MBFP

Mode select : When high, Block Floating Point (BFP) mode is selected. This allows the device to maintain the dynamic range of the data using a series of word tags. This is especially useful in FFT applications. When low, the chip operates in normal mode for more general applications. This pin is intended to be tied high or low, depending on application.

$\overline{\text{SOBFP}}$ (BFP MODE ONLY)

Start of BFP : This input should be held low for the first cycle of the first pass of the BFP calculations (see Fig.7). It serves to reset the internal registers associated with BFP control. When operating in normal mode this input should be tied low.

$\overline{\text{EOPSS}}$ (BFP MODE ONLY)

End of pass: This input should be held low for the last cycle of each pass and for the lay time between passes. It instructs the control logic to update the value of the global weighting register and prepare the BFP circuitry for the next pass. When operating in normal mode this input should be tied low.

AR15:13 (BFP MODE ONLY)

Three msb's of the real part of the A-word : These are used in the FFT butterfly application to determine the magnitude of the real part of the A-word and, hence, to determine if there will be any change of word growth in the PDSP16318 Complex Accumulator. When operating in normal mode, these inputs are not used and may be tied low.

AI15:13 (BFP MODE ONLY)

Three msb's of the imaginary part of the A-word : used in the same fashion as AR.

SFTR2:0 (BFP MODE ONLY)

Accumulator result shift control. These pins should be linked directly to the S2:0 pins on the PDSP16318 Complex Accumulator. They control the accumulator's barrel shifter (see Table 5). The purpose of this shift is to minimise sign extension in the multiplier or accumulator ALU's. When operating in normal mode, these outputs are superfluous.

SFTR2:0	FUNCTION
0 0 0	Reserved
0 0 1	Reserved
0 1 0	Reserved
0 1 1	Shift right by one
1 0 0	No shift
1 0 1	Shift left by one
1 1 0	Shift left by two
1 1 1	Reserved

Table 5 Accumulator Shifts (BFP mode)

GWR4:0 (BFP MODE ONLY)

Contents of the global weighting register: This stores the weighting of the largest word present with respect to the weighting of the original input words. Hence, if the contents of the GWR are 00010, this indicates that the largest word currently being processed has its binary point two bits to the right of the original data at the start of the BFP calculations. The contents of this register are updated at the end of each pass, according to the largest value of WTOUT occurring during that pass. (i.e. If WTOUT = 11, then the GWR will be increased by 2). The GWR is presented in two's complement format. These outputs are superfluous in normal mode.

WTOUT1:0 (BFP MODE ONLY)

Word tag output. This tag records the weighting of the output words from the current cycle relative to the current global weighting register (see Table 6). It should be stored along with the A' and B' words as it will form the input word tags, WTA and WTB, for each complex word during the next pass. These outputs are superfluous in normal mode.

WTOUT1:0	Weighting of the output relative to the current global weighting register
0 0	One less
0 1	The same
1 0	One more
1 1	Two more

Table 6 Word Tag Weightings

WTA1:0 (BFP MODE ONLY)

Word tag from the A-word. This word records the weighting of the A-word relative to the global weighting register on the previous pass. Although the A-word itself is not processed in the PDSP16116, this information is required by the control logic for the radix-2 butterfly FFT application. These inputs should be tied low in normal mode.

WTB1:0 (BFP & NORMAL MODES)

In BFP mode, this is the word tag from the B-word. This is operated in the same manner as WTA but for the B-word. The value of the word tags are used to ensure that the binary weighting of the A word and the product of the complex multiplier are the same at the inputs to the complex accumulator. Depending on which word is the larger, the weighting adjustment is performed using either the internal shifter or an external shifter controlled by SFTA. The word tags are also used to maintain the weighting of the final result to within plus two and minus one binary points relative to the new GWR. (On the first pass all word tags will be ignored).

In normal mode,these inputs perform a different function. They directly control the internal shifter at the output port as shown in Table 7 .

WTB1:0	FUNCTION
11	shift complex product one place to the left
00	no shift applied
01	shift complex product one place to the right
10	shift complex product two places to the right

Table 7 Normal Mode Shift Control

SFTA1:0 (BFP & NORMAL MODES)

In BFP mode, these signals act as the A-word shift control. They allow shifting from one to four places to the right, see Table 8. Depending on the relative weightings of the A-word and the complex product, the A-word may have to be shifted to the right to ensure compatible weightings at the inputs to the PDSP16318 complex accumulator. (The two words must have the same weighting if they are to be added).

In normal mode, SFTA0 performs a different function. If WTB1:0 is set to implement a left shift, then overflow will occur if the data is fully 32 bits wide. This pin is used to flag such an overflow. SFTA1 is not used in normal mode.

SFTA1:0	FUNCTION
0 0	Shift A-word 1 place to the right
0 1	Shift A-word 2 place to the right
1 0	Shift A-word 3 place to the right
1 1	Shift A-word 4 place to the right

Table 8 External A-word shift control

OSEL1:0

The outputs from the device are selected by the OSEL0 & OSEL1 instruction bits. These controls allow selection of the output combination during the current cycle. (They are not registered). There are four possible output configurations that allow either complex outputs of the most or least significant bytes, or real or imaginary outputs of the full 32 bit word (See Table 4). OSEL0 and OSEL1 should both be tied low when in BFP mode.

BFP MODE FFT APPLICATION

The PDSP16116 may be used as the main arithmetic unit of a butterfly processor which will allow the following FFT benchmarks :

1024 point complex radix-2 transform in 517µs
512 point complex radix-2 transform in 235µs
256 point complex radix-2 transform in 106µs

In addition, with pin MBFP tied high, the BFP circuitry within the PDSP16116 can be used to adaptively rescale data throughout the course of the FFT so as to give high-resolution results.

The BFP system on the PDSP16116 can be used with any variation of the Radix-2 Decimation-In-Time FFT - e.g. the Constant Geometry algorithm, the In-Place algorithm etc. An N-point Radix-2 DIT FFT is split into $\log_2(N)$ passes. Each pass consists of N/2 'butterflies', each performing the operation :

$A' = A + B.W$
$B' = A - B.W$

where W is the complex coefficient and A & B are the complex data.

Fig.4 illustrates how a single PDSP16116 may be combined with two PDSP1601's and two PDSP16318s to form a complete BFP butterfly processor. The PDSP16318s are used to perform the complex addition and subtraction of the butterfly operation, while the PDSP1601's are used to match the data path of the A-word to the pipelining and shifting operations within the PDSP16116.

For more information on the theory and construction of this butterfly processor, refer to application note AN59.

BFP MODE OPERATION

The BFP mode on the PDSP16116 is intended for use in the FFT application described above. i.e. it is intended to prevent data degredation during the course of an FFT calculation. The operation of the PDSP16116 based BFP butterfly processor (see Fig.4) is described below.

The Block Floating Point System

A block floating point system is essentially an ordinary integer arithmetic system with some clever logic bolted on. The object of the extra logic is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary weighting. i.e. the binary point should occupy the same position in every data word, as is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited. In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point within the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point available, each denoted by a certain value of word tag :

XX.XXXXXXXXXXXXX word tag = 00
XXX.XXXXXXXXXXXX word tag = 01
XXXX.XXXXXXXXXXX word tag = 10
XXXXX.XXXXXXXXXX word tag = 11

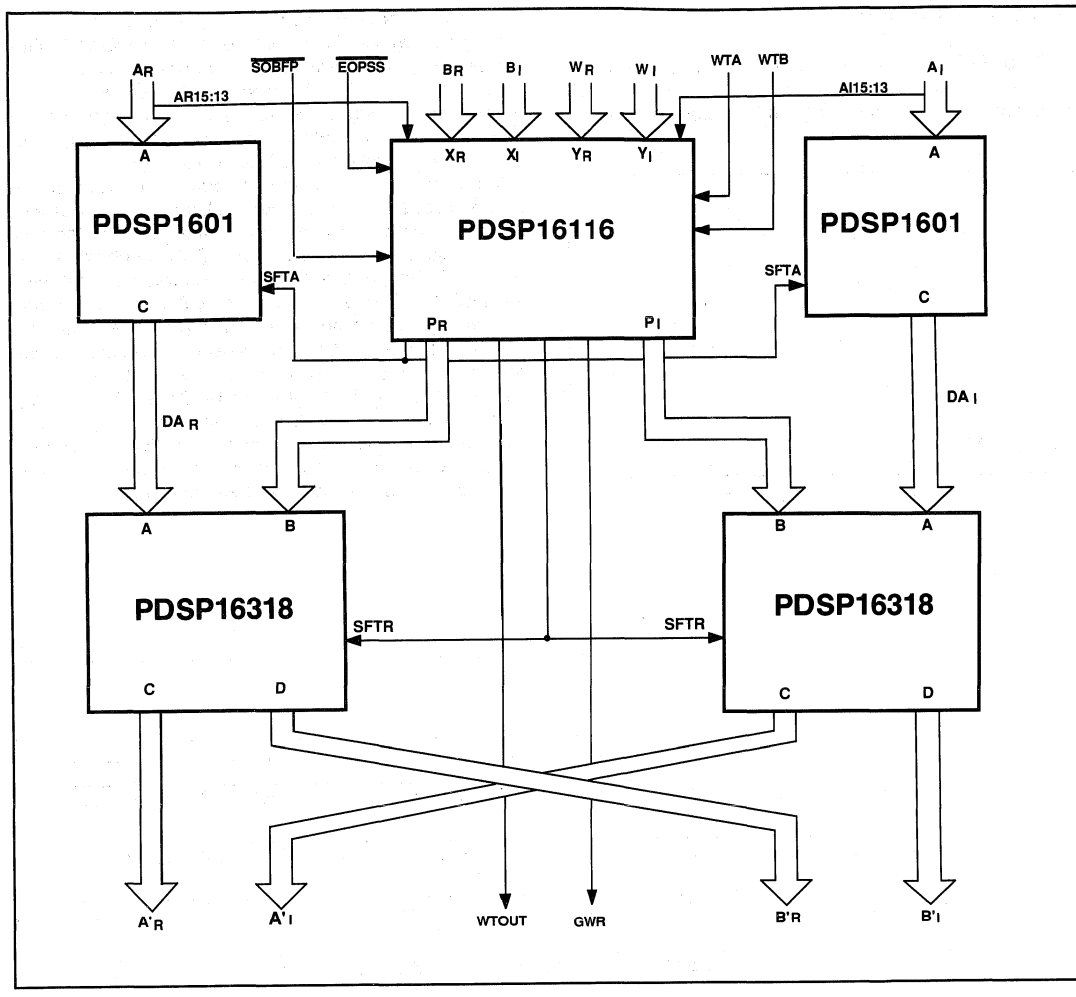


Fig. 4 FFT Butterfly Processor

At the end of each constituent pass of the FFT, the positions of the binary points supported may change to reflect the trend of data increases or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may change to :

XXXX.XXXXXXXXXXX	word tag = 00
XXXXX.XXXXXXXXXX	word tag = 01
XXXXXX.XXXXXXXXX	word tag = 10
XXXXXXX.XXXXXXXX	word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the GWR.

-Thus we can determine the position of the binary point relative to its initial position by modifying the value of GWR by WTOUT for a given word as shown in Table 6.

As an example, if GWR=01001 and WTOUT=10 then the binary point has moved 10 places to the right of its original position.

The Butterfly Operation

The butterfly operation is the arithmetic operation which is repeated many times to produce an FFT. The PDSP16116 based butterfly processor performs this operation in a low power high accuracy chip set.

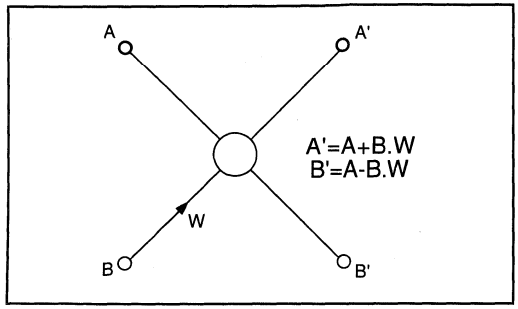


Fig. 5 Butterfly Operation

A new butterfly operation is commenced each cycle, requring a new set of data for A, B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601 and PDSP16318. The timing of the data and control signals is shown in Fig.6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. Each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A' and B', it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A-word is known as WTA and the word tag associated with the B-word is known as WTB. Hence, the WTOUT's from one pass will become the WTA's and WTB's for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data initially has the same weighting. Hence, during the first pass alone, the inputs WTA and WTB are ignored.

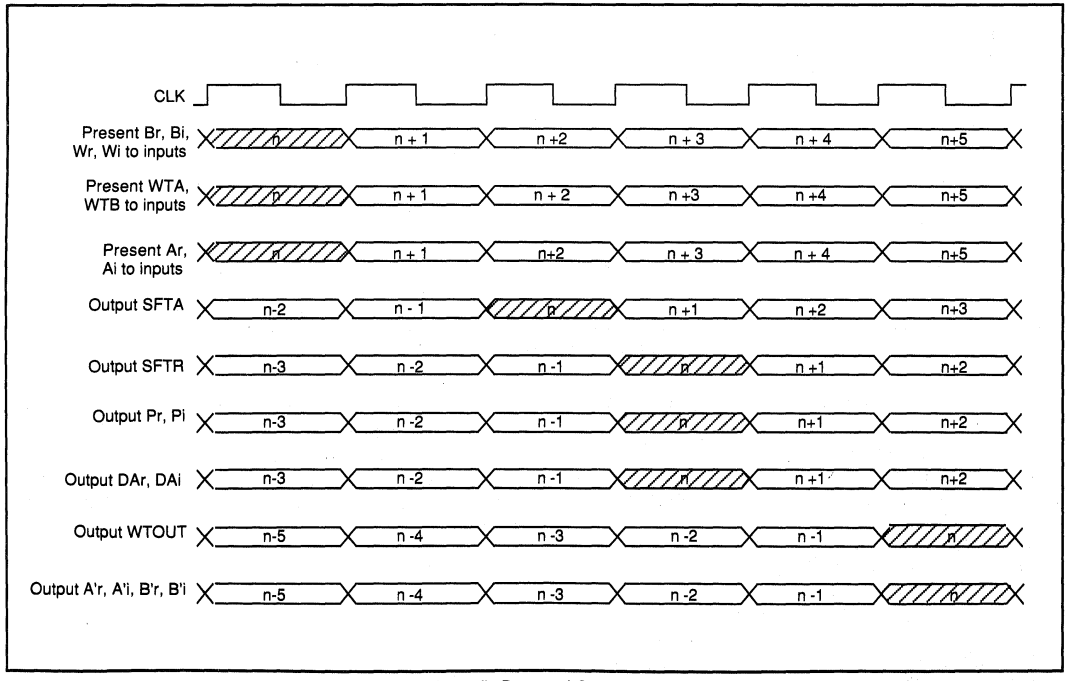


Fig. 6 Butterfly Data and Control Signals

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided :

$\overline{SOBFP}$ - start of the FFT

$\overline{EOPSS}$ - end of current pass

These inform the PDSP16116 when an FFT is starting and when each pass is complete. Fig.7 shows how these signals should be used and a commentary is provided below.

To commence the FFT, the signal $\overline{EOPSS}$ should be set high (where it will remain for the duration of the pass). $\overline{SOBFP}$ should be pulled low during the initial cycle when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle $\overline{SOBFP}$ must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal $\overline{EOPSS}$ should be pulled low and remain low for a minimum of five cycles *, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass. On the initial cycle of each new pass, the signal $\overline{EOPSS}$ should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

* Should a longer pause` be required between passes - to arrange the data for the next pass, for example, then $\overline{EOPSS}$ may be kept low as long as necessary - the next pass cannot commence until it is brought high again.

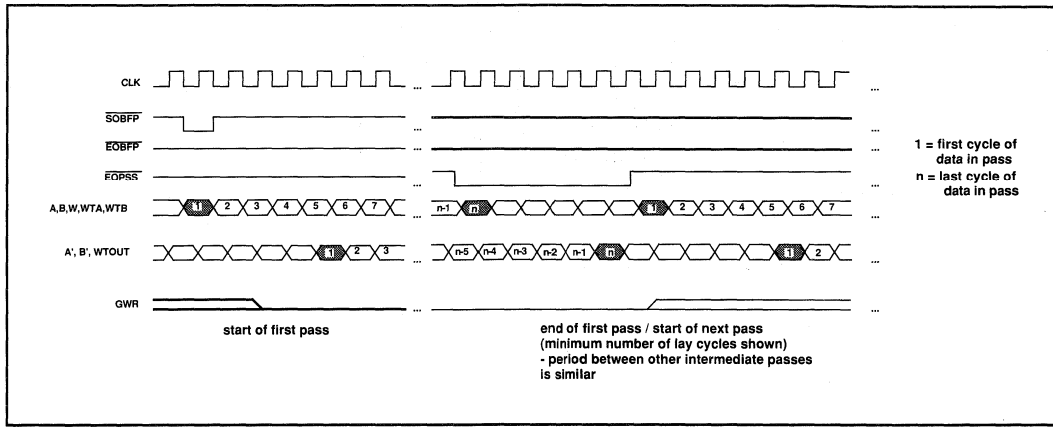


Fig. 7 Use of the BFP Control Signals

FFT Output Normalisation

When an FFT system outputs a series of FFT results for display, storage or transmission, it is essential that all results are compatible, i.e. with the binary point in the same position. However, in order to preserve the dynamic range of the data in the FFT calculation, the PDSP16116 employs a range of different weightings. Therefore, data must be re-formatted at the end of the FFT to a pre-determined common weighting. This can be done by comparing the exponent of a given data word with the pre-determined universal exponent and then shifting the data word by the difference. The PDSP1601, with its multifunction 16 bit barrel shifter, is ideally suited to this task.

What value should the Universal Exponent take ? Well, according to theory, the largest possible data result from an FFT is N times the largest input data. This means that the binary point can move a maximum of log2(N) places to the right. Hence, if we choose the Universal Exponent to be log2(N) this should give us sufficient range to represent all data points faithfully.

In practice, data output may never approach the theoretical maximum. Hence, it may be worthwhile to try various Universal Exponents and choose the one best suited to the particular application.

Data is output from the butterfly processor with a two-part exponent : the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by its WTOUT as shown in Table 6. The result is the number of places the binary point has been shifted to the right during the course of the FFT.

This value must be compared with the Universal Exponent to determine the shift required. This is done by subtracting it from the Universal Exponent. The number of places to be shifted is equal to the difference between the two exponents. The shift can be implemented in a PDSP1601. The shift value is fed into the SV port.

As FFT data consists of real and imaginary parts, either two PDSP1601's must be used (controlled by the same logic) or a single PDSP1601 could be used handling real and imaginary data on alternate cycles (using the same instructions for both cycles).

An example of an output normalisation circuit is shown in Fig.8. Only 4 bit data paths are used in calculating the shift. This means that we must be able to trap very small values (-ve) of GWR and force a 15-bit right shift in such cases.

N.B.

It is easier to simply add the word tag to the exponent for the purposes of determining the shift required, instead of modifying it according toTable 6. To compensate for this, the Universal Exponent may be increased by one.

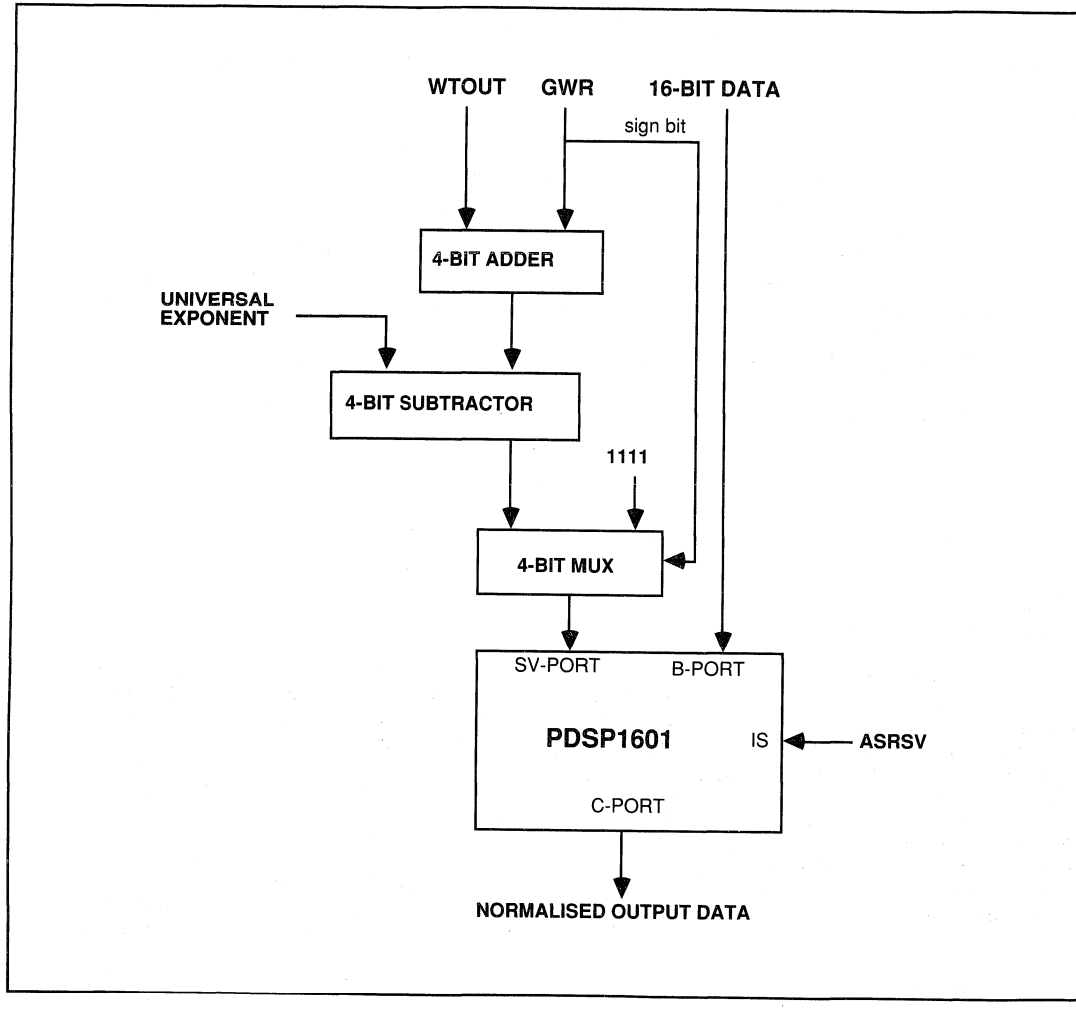


Fig. 8 Output Normalisation Circuitry

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to Vcc + 0.9V
Output voltage V_{OUT}	-0.9V to Vcc + 0.9V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	
Military	-55°C to +125°C
Industrial	-40°C to 85°C
Junction temperature	150°C
Package power dissipation	1000mW
Thermal resistances	
Junction to case $ø_{JC}$	12°C/W
Junction to ambient $ø_{JA}$	29°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.

ELECTRICAL CHARATERISTICS

Operating Conditions (unless otherwise stated)

Industrial: Tamb = -40°C to +85°C Vcc = 5.0V±10% Ground = 0V
Military: Tamb = -55°C to +125°C Vcc = 5.0V±10% Ground=0V

Static Characteristics

Charateristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 8mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -8mA
Input high voltage	V_{IH}	2.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IL}	-5		-5	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-10		+10	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{CC}	10		100	mA	V_{CC} = Max

Switching Characteristics

Charateristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CLK rising edge to P-PORTS	-	40		ns	2 x LSTTL + 20pF
CLK rising edge to WTOUT1:0	-	25		ns	2 x LSTTL + 20pF
CLK rising edge to GWR4:0	-	25		ns	2 x LSTTL + 20pF
CLK rising edge to SFTA1:0	-	35		ns	2 x LSTTL + 20pF
CLK rising edge to SFTR2:0	-	40		ns	2 x LSTTL + 20pF
Setup $\overline{CEX}$ or $\overline{CEY}$ to CLK rising edge		10	-	ns	
Hold $\overline{CEX}$ or $\overline{CEY}$ to CLK rising edge	-		0	ns	
Setup X or Y port inputs to CLK rising edge		10	-	ns	
Hold X or Y port inputs to clock rising edge	-		0	ns	
Setup WTA1:0, WTB1:0, $\overline{SOBFP}$ or $\overline{EOPSS}$ inputs to CLK rising edge		10	-	ns	
Hold WTA1:0, WTB1:0, $\overline{SOBFP}$ or $\overline{EOPSS}$ inputs to CLK rising edge	-		0	ns	
Setup CONX or CONY inputs to CLK rising edge		10	-	ns	
Hold CONX or CONY inputs to CLK rising edge	-		0	ns	
Setup AR15:13 or AI15:13 to CLK rising edge		10	-	ns	
Hold AR15:13 or AI15:13 to CLK rising edge	-		0	ns	
OPSEL to valid P-PORTS		40	-	ns	2 x LSTTL + 20pF
$\overline{OER}$ or $\overline{OEI}$ risingPR-PORT or PI-PORT high to Z	-		45	ns	see Fig. 8
$\overline{OER}$ or $\overline{OEI}$ risingPR-PORT or PI-PORT low to Z	-		45	ns	see Fig. 8
$\overline{OER}$ or $\overline{OEI}$ fallingPR-PORT or PI-PORT Z to high	-		45	ns	see Fig. 8
$\overline{OER}$ or $\overline{OEI}$ fallingPR-PORT or PI-PORT Z to low	-		45	ns	see Fig. 8
Clock period	100		-	ns	
Clock high time	20		-	ns	
Clock low time	20		-	ns	
Vcc Current (CMOS input levels)	-	80		mA	Note 4
Vcc Current (TTL input levels)	-	100		mA	Note 4

NOTE 4 :- V_{CC} = Max, Outputs unloaded, Clock freq = Max

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H 0.5V
Delay from output low to output high impedance	V_L 0.5V
Delay from output high impedance to output low	1.5V 0.5V
Delay from output high impedance to output high	1.5V 0.5V

V_H - Voltage reached when output driven high
V_L - Voltage reached when output driven low

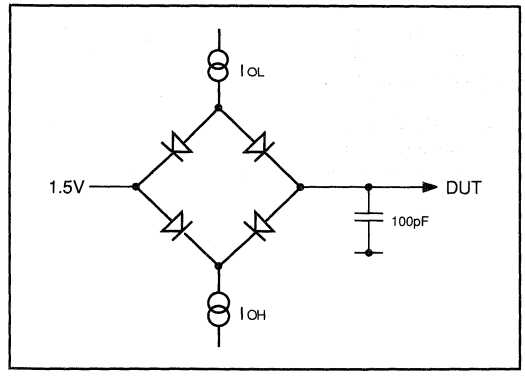
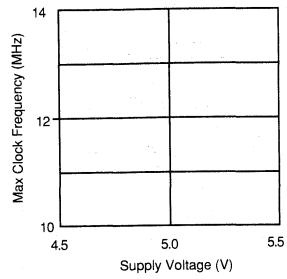
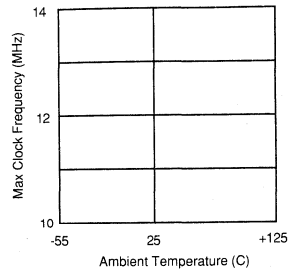


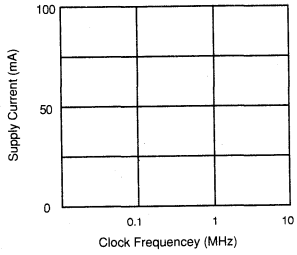
Fig. 9 Three state delay measurment load.



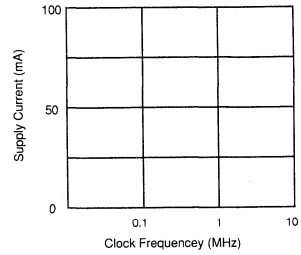
Variation in Max Clock frequency over supply voltage



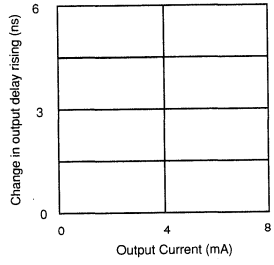
Variation in Max Clock frequency over temperature



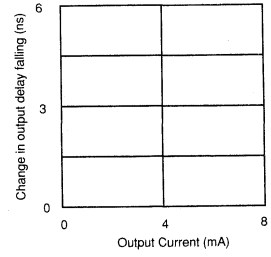
Variation in supply current with clock frequency (TTL input levels)



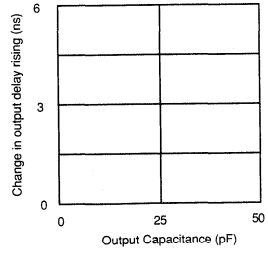
Variation in supply current with clock frequency (CMOS input levels)



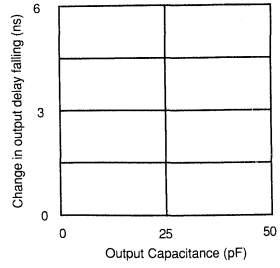
Variation in output rising delay with output current



Variation in output falling delay with output current



Variation in output falling delay with output capacitance



Variation in output falling delay with output capacitance

ORDERING INFORMATION

PDSP16116 B0 AC Industrial
PDSP16116 A0 AC Military

Call for availability on High Reliability parts and MIL-883C screening.

PLESSEY
Semiconductors

PDSP16316/PDSP16316A

COMPLEX ACCUMULATOR

The PDSP16316 contains two independent 20-bit Adder/Subtractors combined with accumulator registers and shift structures. The four port architecture permits full 20MHz throughput in FFT and filter applications.

Two PDSP16316As combined with a single PDSP16112A Complex Multiplier provide a complete arithmetic solution for a Radix 2 DIT FFT Butterfly. A new complex Butterfly result can be generated every 50ns allowing 1K complex FFT's to be executed in 256μs.

FEATURES

- Full 20MHz Throughput in FFT Applications
- Four Independent 16-bit I/O Ports
- 20-bit Addition or Accumulation
- Two's Complement Fractional Arithmetic
- Full Compatible with PDSP16112 Complex Multiplier
- On Chip Shift Structures for Result Scaling
- Overflow Detection
- Independent Three-State Outputs and Clock Enables for 2 Port 20MHz Operation
- 2 micron CMOS
- 500mW Maximum Power Dissipation
- 84 Pin PGA Package

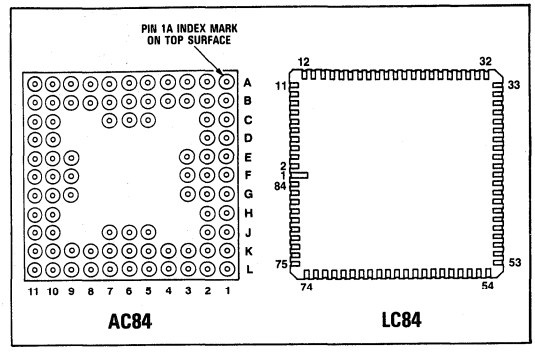


Fig.1 Pin connections - bottom view

APPLICATIONS

- High Speed Complex FFT or DFT's
- Complex Finite Impulse Response (FIR) Filtering
- Complex Conjugation
- Complex Correlation/Convolution

ASSOCIATED PRODUCTS

PDSP16112 16 x 12 Complex Multiplier
PDSP1601 Arithmetic Logic Unit
PDSP1640 40MHz Address Generator
PDSP16330 Pythagoras Processor
PDSP16116 16 x 16 Complex Multiplier

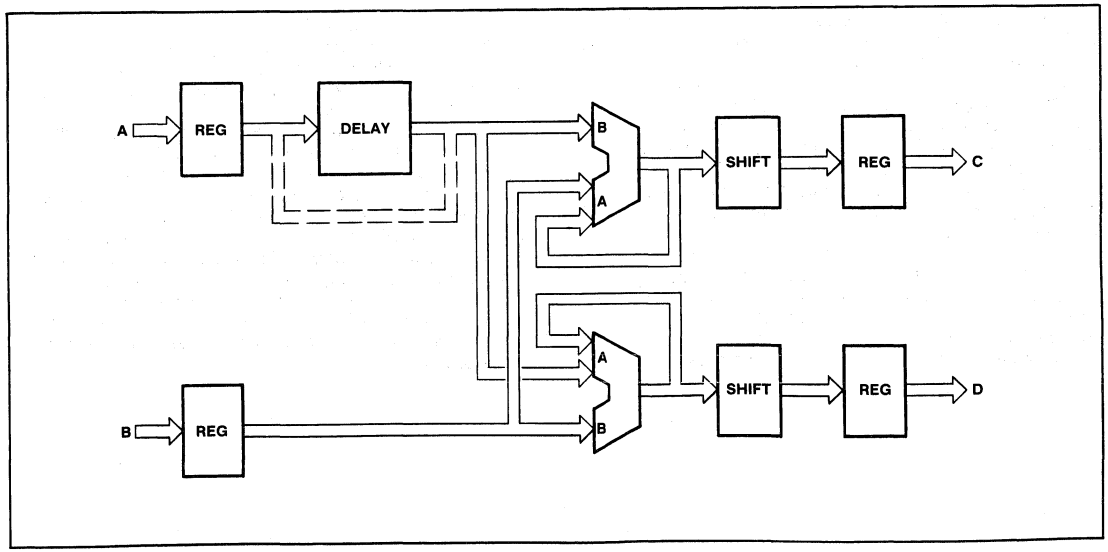


Fig.2 PDSP16316 simplified block diagram

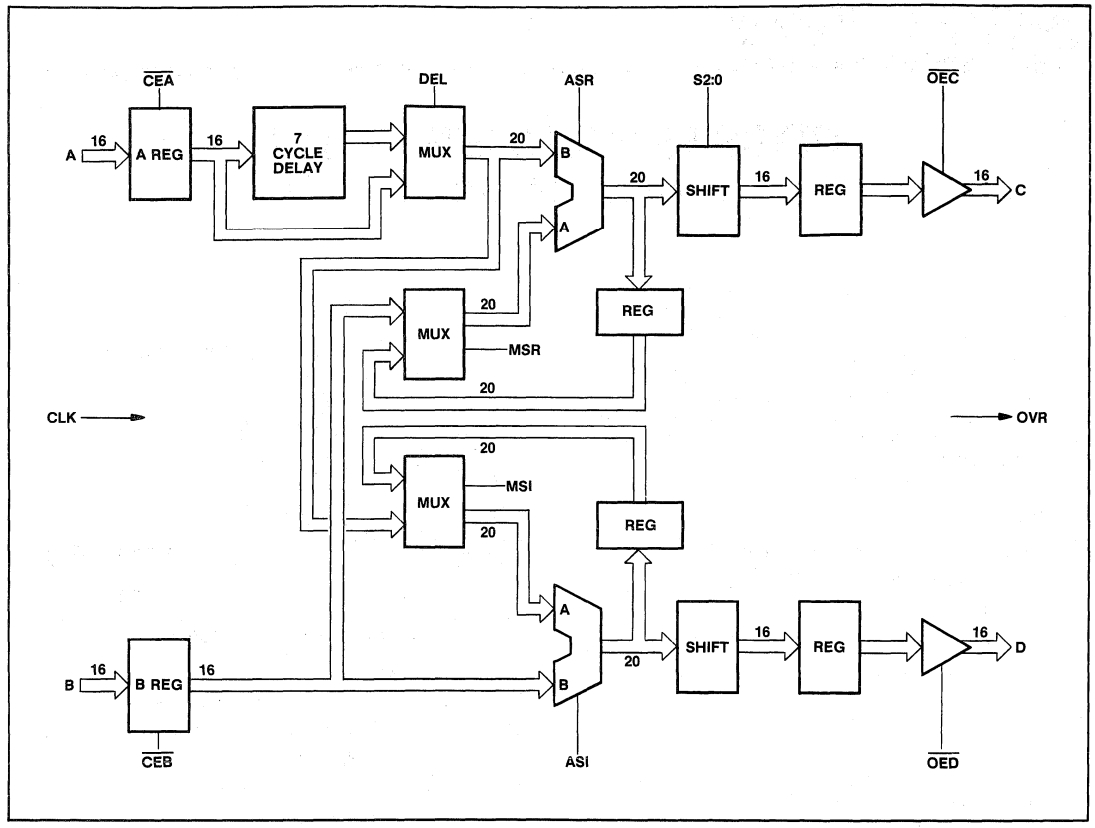


Fig.3 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16316 is a Dual 20-bit Adder/Subtractor configured to support Complex Arithmetic. The device may be used with each of the adders allocated to real or imaginary data (e.g. Complex Conjugation), the entire device allocated to Real or Imaginary Data (e.g. Radix 2 Butterflys) or each of the adders configured as accumulators and allocated to real or imaginary data (Complex Filters). Each of these modes ensures that a full 20MHz throughput is maintained through both adders, the first and last mode illustrating true Complex operation, where both real and imaginary data is handled by the single device.

Both Adder/Subtractors may be controlled independently via the ASR and ASI inputs. These controls permit A + B, A - B, B - A or pass A operations, where the A input to the Adder is derived from the input multiplixer. Each of the two multiplexers may be controlled independently via the MSR and MSI inputs, to select either new input data, or fed-back data from the accumulator registers. The PDSP16316 contains a 7 cycle deskew register selected via the DEL control. This deskew register is used in FFT applications to ensure correct phasing of data that has not passed through the PDSP16112 Complex Multiplier.

The 16-bit outputs from the PDSP16316 are derived from the 20-bit result generated by the Adders. The three bit S2:0 input selects eight different shifted output formats ranging from the most significant 16 bits of the 20-bit data, to the least significant 13 bits of the 20-bit data. In this mode the 14th, 15th and 16th bits of the output are set to zero. The shift selected is applied to both adder outputs, and determines the function of the OVR flag. The OVR flag becomes active when either of the two adders produces a result that has more significant digits than the MSB of the 16-bit output from the device. In this manner all cases when invalid data appears on the output are flagged.

PIN DESCRIPTIONS

Symbol	Type	Description
A15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. A15 is the MSB.
B15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. B15 is the MSB and has the same weighting as A15.
C15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
D15:0	Output	New **data** appears on this output after the rising edge of CLK. D15 is the MSB.
CLK	Input	**Common Clock** to all internal registers
$\overline{CEA}$	Input	**Clock enable:** when low the clock to the A input register is enabled.
$\overline{CEB}$	Input	**Clock enable:** when low the clock to the B input register is enabled.
$\overline{OEC}$	Input	**Output enable:** Asynchronous 3-state output control: The C outputs are in a high impedance state when this input is high.
$\overline{OED}$	Input	**Output enable:** Asynchronous 3-state output control: The D outputs are in a high impedance state when this input is high.
OVR	Output	**Overflow flag:** This flag will go high in any cycle during which either the output data overflows the number range selected or either of the adder results overflow. A new OVR appears after the rising edge of the CLK.
ASR1:0	Input	**Add/subtract Real:** Control input for the 'Real' adder. This input is latched by the rising edge of clock.
ASI1:0	Input	**Add/subtract Imag:** Control input for the 'Imag' adder. This input is latched by the rising edge of clock.
MSR	Input	**Mux select Real:** Control input for the 'Real' adder mux. This input is latched by the rising edge of CLK. When high the feedback path is selected.
MSI	Input	**Mux select Imag:** Control input for the 'Imag' adder mux. This input is latched by the rising edge of CLK. When high the feedback path is selected.
S2:0	Input	**Scaling control:** This input selects the 16-bit field from the 20-bit adder result that is routed to the outputs. This input is latched by the rising edge of CLK.
DEL	Input	**Delay Control:** This input selects the delayed input to the real adder for operations involving the PDSP16112. This input is latched by the rising edge of CLK.
VCC	Power	**+5V supply:** Both Vcc pins must be connected.
GND	Ground	**0V supply:** Both GND pins must be connected.

LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function	LC Pin	AC Pin	Function
75	B2	D7	12	K2	C7	33	K10	A1	54	B10	B10
76	C2	D8	13	K3	C6	34	J10	A2	55	B9	B9
77	B1	D9	14	L2	C5	35	K11	A3	56	A10	B8
78	C1	D10	15	L3	C4	36	J11	A4	57	A9	B7
79	D2	GND	16	K4	C3	37	H10	A5	58	B8	B6
80	D1	Vcc	17	L4	C2	38	H11	A6	59	A8	B5
81	E3	D11	18	J5	C1	39	F10	A7	60	B6	B4
82	E2	D12	19	K5	C0	40	G10	A8	61	B7	B3
83	E1	D13	20	L5	$\overline{OED}$	41	G11	A9	62	A7	B2
84	F2	D14	21	K6	$\overline{OEC}$	42	G9	A10	63	C7	B1
1	F3	D15	22	J6	S2	43	F9	A11	64	C6	B0
2	G3	C15	23	J7	S1	44	F11	A12	65	A6	CLK
3	G1	C14	24	L7	S0	45	E11	A13	66	A5	$\overline{CEB}$
4	G2	C13	25	K7	MSI	46	E10	A14	67	B5	OVR
5	F1	C12	26	L6	ASI1	47	E9	A15	68	C5	D0
6	H1	Vcc	27	L8	ASI0	48	D11	$\overline{CEA}$	69	A4	D1
7	H2	GND	28	K8	DEL	49	D10	B15	70	B4	D2
8	J1	C11	29	L9	MSR	50	C11	B14	71	A3	D3
9	K1	C10	30	L10	ASR1	51	B11	B13	72	A2	D4
10	J2	C9	31	K9	ASR0	52	C10	B12	73	B3	D5
11	L1	C8	32	L11	A0	53	A11	B11	74	A1	D6

ASR or ASI ASX1	ASX0	ALU Function
0	0	A + B
0	1	A
1	0	A - B
1	1	B - A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MSR	Real Mux Control
0	B port input
1	C accumulator

MSI	Imag' Mux Control
0	Del mux output
1	D accumulator

S2:0			Adder result																	
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3	2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4	3

NOTE
This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected, the output data is padded with zeros.

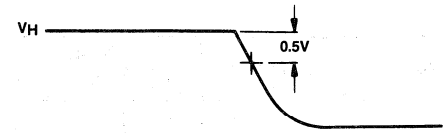
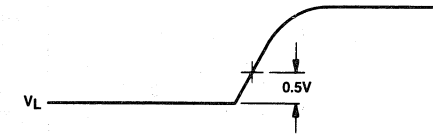
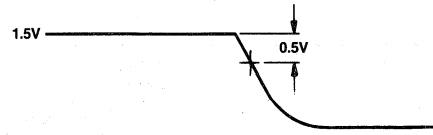
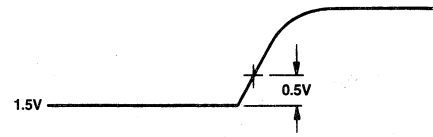
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

NOTES
1. V_H - Voltage reached when output driven high.
2. V_L - Voltage reached when output driven low.

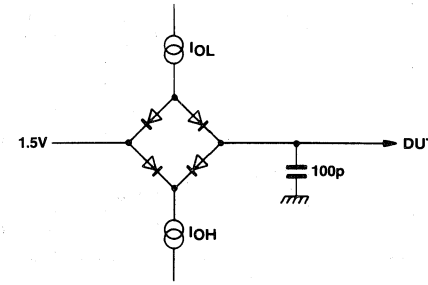


Fig.4 Three state delay measurement load

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -3.2mA
Input high voltage	V_{IH}	2.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IL}	-5		+5	μA	GND ≤ V_{IN} ≤ V_{CC}
Input capacitance	C_{IN}	-	-	5	pF	
Output leakage current	I_{OZ}	-10	-	+10	μA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	10	-	100	mA	V_{CC} = Max
Input capacitance	C_I	-	9		pF	

Switching Characteristics

Characteristic	Value Industrial						Value Military		Units	Conditions
	PDSP16316			PDSP16316A						
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Max.		
Clock period	100		-	50		-	100		ns	
Clock high time	20		-	15		-	20		ns	
Clock low time	20		-	15		-	20		ns	
A15:0, B15:0 setup to clock rising edge	8		-	5		-	8		ns	
A15:0, B15:0 hold after clock rising edge	8		-	5		-	8		ns	
DEL, ASR, ASI, MSR, MSI, S2:0 setup to clock rising edge	10		-	5		-	10		ns	
DEL, ASR, ASI, MSR, MSI, S2:0 hold after clock rising edge	10		-	6		-	10		ns	
$\overline{CEA}$, $\overline{CEB}$ setup to clock falling edge	0		-	0		-	0		ns	
$\overline{CEA}$, $\overline{CEB}$ hold after clock rising edge	0		-	0		-	0		ns	
Clock rising edge to OVR, C15:0, D15:0	-		40	-		30		40	ns	2 x LSTTL +20pF
$\overline{OEC}$ low to C15:0 high data valid	-		40	-		30		40	ns	
$\overline{OEC}$ low to C15:0 low data valid	-		40	-		30		40	ns	
$\overline{OEC}$ high to C15:0 high impedance	-		40	-		30		40	ns	
$\overline{OED}$ low to D15:0 high data valid	-		40	-		30		40	ns	
$\overline{OED}$ low to D15:0 low data valid	-		40	-		30		40	ns	
$\overline{OED}$ high to D15:0 high impedance	-		40	-		30		40	ns	
V_{CC} current	-		50	-		100		50	mA	V_{CC} = max Outputs unloaded f_{CLK} = max

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16316 B0 AC **PDSP16316 B0 LC**
PDSP16316A BO AC **PDSP16316A B0 LC**

Military (-55°C to +125°C)

PDSP16316 A0 AC **PDSP16316 A0 LC**

Call for availability on High Reliability parts and MIL 883C screening.

PDSP16318/PDSP16318A
COMPLEX ACCUMULATOR

The PDSP16318 contains two independent 20-bit Adder/Subtractors combined with accumulator registers and shift structures. The four port architecture permits full 20MHz throughput in FFT and filter applications.

Two PDSP16318As combined with a single PDSP16112A Complex Multiplier provide a complete arithmetic solution for a Radix 2 DIT FFT Butterfly. A new complex Butterfly result can be generated every 50ns allowing 1K complex FFT's to be executed in 256μs.

The PDSP16318/A is recommended for new designs instead of PDSP16316/A.

FEATURES

- Full 20MHz Throughput in FFT Applications
- Four Independent 16-bit I/O Ports
- 20-bit Addition or Accumulation
- Fully Compatible with PDSP16112 Complex Multiplier
- On Chip Shift Structures for Result Scaling
- Overflow Detection
- Independent Three-State Outputs and Clock Enables for 2 Port 20MHz Operation
- 1.5 micron CMOS
- 500mW Maximum Power Dissipation
- 84 Pin PGA Package

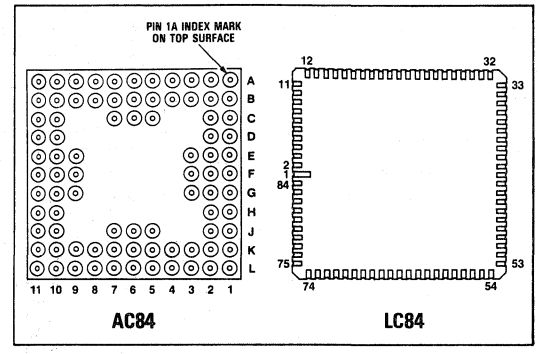


Fig.1 Pin connections - bottom view

APPLICATIONS

- High Speed Complex FFT or DFT's
- Complex Finite Impulse Response (FIR) Filtering
- Complex Conjugation
- Complex Correlation/Convolution

ASSOCIATED PRODUCTS

PDSP16112 16 x 12 Complex Multiplier
PDSP16116 16 x 16 Complex Multiplier
PDSP1601 Arithmetic Logic Unit/Barrel Shifter
PDSP1640 40MHz Address Generator
PDSP16330 Pythagoras Processor

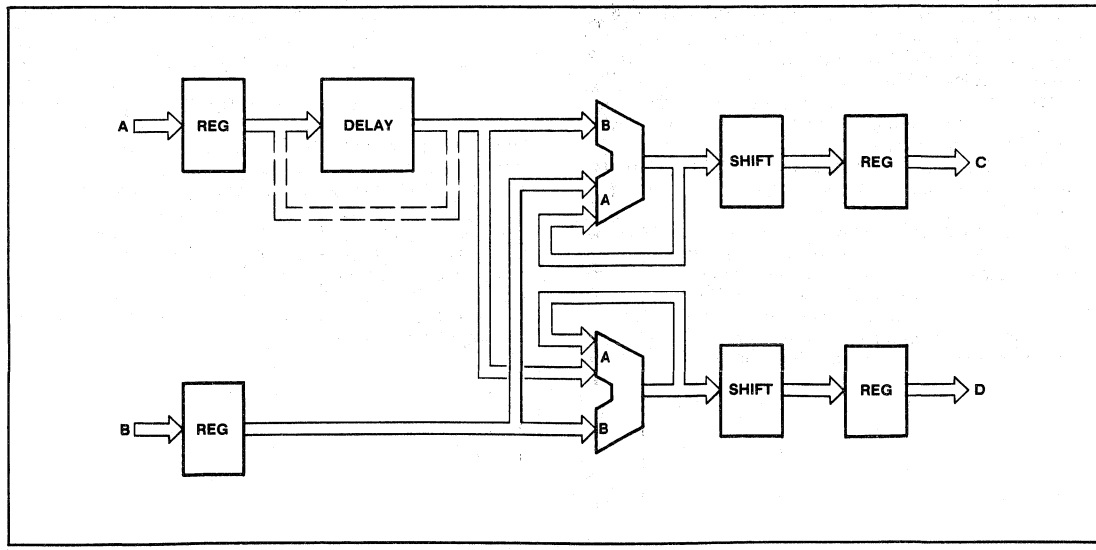


Fig.2 PDSP16318 simplified block diagram

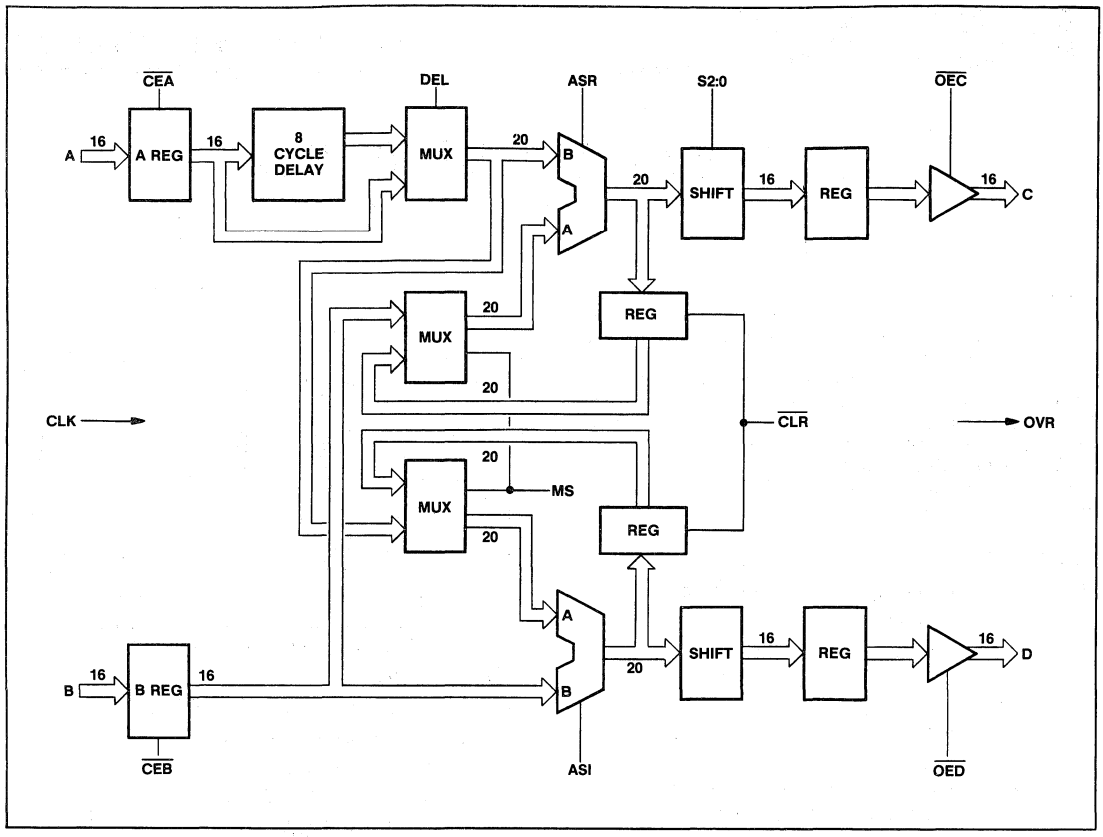


Fig.3 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16318 is a Dual 20-bit Adder/Subtractor configured to support Complex Arithmetic. The device may be used with each of the adders allocated to real or imaginary data (e.g. Complex Conjugation), the entire device allocated to Real or Imaginary Data (e.g. Radix 2 Butterflys) or each of the adders configured as accumulators and allocated to real or imaginary data (Complex Filters). Each of these modes ensures that a full 20MHz throughput is maintained through both adders, the first and last mode illustrating true Complex operation, where both real and imaginary data is handled by the single device.

Both Adder/Subtractors may be controlled independently via the ASR and ASI inputs. These controls permit A + B, A - B, B - A or pass A operations, where the A input to the Adder is derived from the input multiplexer. The $\overline{CLR}$ control line allows the clearing of both accumulator registers.The two multiplexers may be controlled via the MS inputs, to select either new input data, or fed-back data from the accumulator registers. The PDSP16318 contains an 8-cycle deskew register selected via the DEL control. This deskew register is used in FFT applications to ensure correct phasing of data that has not passed through the PDSP16112 Complex Multiplier.

The 16-bit outputs from the PDSP16318 are derived from the 20-bit result generated by the Adders. The three bit S2:0 input selects eight different shifted output formats ranging from the most significant 16 bits of the 20-bit data, to the least significant 13 bits of the 20-bit data. In this mode the 14th, 15th and 16th bits of the output are set to zero. The shift selected is applied to both adder outputs, and determines the function of the OVR flag. The OVR flag becomes active when either of the two adders produces a result that has more significant digits than the MSB of the 16-bit output from the device. In this manner all cases when invalid data appears on the output are flagged.

PIN DESCRIPTIONS

Symbol	Type	Description
A15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. A15 is the MSB.
B15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. B15 is the MSB and has the same weighting as A15.
C15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
D15:0	Output	New **data** appears on this output after the rising edge of CLK. D15 is the MSB.
CLK	Input	**Common Clock** to all internal registers
$\overline{CEA}$	Input	**Clock enable:** when low the clock to the A input register is enabled.
$\overline{CEB}$	Input	**Clock enable:** when low the clock to the B input register is enabled.
$\overline{OEC}$	Input	**Output enable:** Asynchronous 3-state output control: The C outputs are in a high impedance state when this input is high.
$\overline{OED}$	Input	**Output enable:** Asynchronous 3-state output control: The D outputs are in a high impedance state when this input is high.
OVR	Output	**Overflow flag:** This flag will go high in any cycle during which either the output data overflows the number range selected or either of the adder results overflow. A new OVR appears after the rising edge of the CLK.
ASR1:0	Input	**Add/subtract Real:** Control input for the 'Real' adder. This input is latched by the rising edge of clock.
ASI1:0	Input	**Add/subtract Imag:** Control input for the 'Imag' adder. This input is latched by the rising edge of clock.
$\overline{CLR}$	Input	**Accumulator Clear:** Common accumulator clear for both Adder/Subtractor units. This input is latched by the rising edge of CLK.
MS	Input	**Mux select:** Control input for both adder multiplexers. This input is latched by the rising edge of CLK. When high the feedback path is selected.
S2:0	Input	**Scaling control:** This input selects the 16-bit field from the 20-bit adder result that is routed to the outputs. This input is latched by the rising edge of CLK.
DEL	Input	**Delay Control:** This input selects the delayed input to the real adder for operations involving the PDSP16112. This input is latched by the rising edge of CLK.
VCC	Power	**+5V supply:** Both Vcc pins must be connected.
GND	Ground	**0V supply:** Both GND pins must be connected.

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
B2	D7	J1	C11	K7	MS	G9	A10	A8	B5
C2	D8	K1	C10	L6	ASI1	F9	A11	B6	B4
B1	D9	J2	C9	L8	ASI0	F11	A12	B7	B3
C1	D10	L1	C8	K8	$\overline{DEL}$	E11	A13	A7	B2
D2	GND	K2	C7	L9	$\overline{CLR}$	E10	A14	C7	B1
D1	Vcc	K3	C6	L10	ASR1	E9	A15	C6	B0
E3	D11	L2	C5	K9	ASR0	D11	$\overline{CEA}$	A6	CLK
E2	D12	L3	C4	L11	A0	D10	B15	A5	$\overline{CEB}$
E1	D13	K4	C3	K10	A1	C11	B14	B5	OVR
F2	D14	L4	C2	J10	A2	B11	B13	C5	D0
F3	D15	J5	C1	K11	A3	C10	B12	A4	D1
G3	C15	K5	C0	J11	A4	A11	B11	B4	D2
G1	C14	L5	$\overline{OED}$	H10	A5	B10	B10	A3	D3
G2	C13	K6	$\overline{OEC}$	H11	A6	B9	B9	A2	D4
F1	C12	J6	S2	F10	A7	A10	B8	B3	D5
H1	Vcc	J7	S1	G10	A8	A9	B7	A1	D6
H2	GND	L7	S0	G11	A9	B8	B6		

ASR or ASI ASX1	ASX0	ALU Function
0	0	A + B
0	1	A
1	0	A - B
1	1	B - A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MS	Real and Imag' Mux Control
0	B port input/Del mux output
1	C accumulator/D accumulator

S2:0			Adder result																	
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3	2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4	3

NOTE
This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected, the output data is padded with zeros.

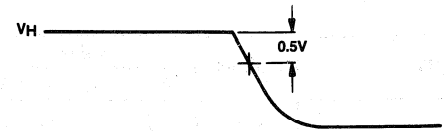
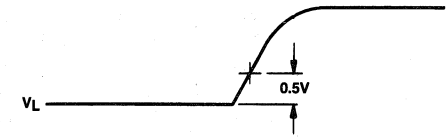
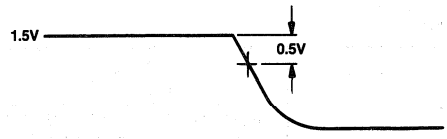
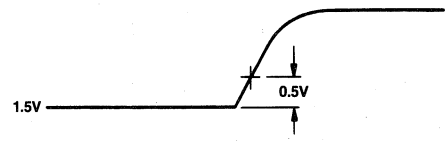
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

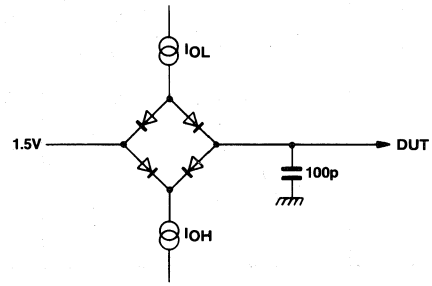
NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

NOTES
1. V_H - Voltage reached when output driven high.
2. V_L - Voltage reached when output driven low.



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V
T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -3.2mA
Input high voltage	V_{IH}	2.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IL}	-5		+5	μA	GND ≤ V_{IN} ≤ V_{CC}
Input capacitance	C_{IN}	-	-	5	pF	
Output leakage current	I_{OZ}	-10	-	+10	μA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	10	-	100	mA	V_{CC} = Max
Input capacitance	C_I	-	9		pF	

Switching Characteristics

Characteristic	Value Industrial						Value Military		Units	Conditions
	PDSP16318			PDSP16318A						
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Max.		
Clock period	100		-	50		-	100		ns	
Clock high time	20		-	15		-	20		ns	
Clock low time	20		-	15		-	20		ns	
A15:0, B15:0 setup to clock rising edge	8		-	5		-	8		ns	
A15:0, B15:0 hold after clock rising edge	8		-	5		-	8		ns	
DEL, ASR, ASI, MS, $\overline{CLR}$, S2:0 setup to clock rising edge	10		-	5		-	10		ns	
DEL, ASR, ASI, MS, $\overline{CLR}$, S2:0 hold after clock rising edge	10		-	6		-	10		ns	
$\overline{CEA}$, $\overline{CEB}$ setup to clock falling edge	0		-	0		-	0		ns	
$\overline{CEA}$, $\overline{CEB}$ hold after clock rising edge	0		-	0		-	0		ns	
Clock rising edge to OVR, C15:0, D15:0	-		40	-		30		40	ns	2 x LSTTL +20pF
$\overline{OEC}$ low to C15:0 high data valid	-		40	-		30		40	ns	
$\overline{OEC}$ low to C15:0 low data valid	-		40	-		30		40	ns	
$\overline{OEC}$ high to C15:0 high impedance	-		40	-		30		40	ns	
$\overline{OED}$ low to D15:0 high data valid	-		40	-		30		40	ns	
$\overline{OED}$ low to D15:0 low data valid	-		40	-		30		40	ns	
$\overline{OED}$ high to D15:0 high impedance	-		40	-		30		40	ns	
V_{CC} current	-		50	-		100		50	mA	V_{CC} = max Outputs unloaded f_{CLK} = max

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16318 B0 AC **PDSP16318 B0 LC**
PDSP16318A BO AC **PDSP16318A B0 LC**

Military (-55°C to +125°C

00**PDSP16318 A0 AC** **PDSP16318 A0 LC**

Call for availability on High Reliability parts and MIL 883C screening.

PLESSEY
Semiconductors

PDSP16330/PDSP16330A

PYTHAGORAS PROCESSOR

(SUPERSEDES OCTOBER 1987 EDITION)

The PDSP16330 is a high speed digital CMOS IC that converts Cartesian data (Real and Imaginary) into Polar form (Magnitude and Phase), at a full 10MHz rate. Cartesian 16 + 16 bit two's complement or Sign Magnitude data is converted into 16 Bit Magnitude and 12 Bit Phase format. The Magnitude output may be scaled in amplitude by powers of 2. The Phase output represents a full $2 \times \pi$ field to eliminate phase ambiguities.

FEATURES

- 15MHz Cartesian to Polar Conversion
- 16-bit Cartesian Inputs
- 16-bit Magnitude Output
- 12-bit Phase Output
- Twos Complement or Sign-Magnitude Input Formats
- Three-state Outputs and Independent Data Enables Simplify System Interfacing
- Magnitude Scaling Facility with Overflow Flag
- Less than 500mW Power Dissipation at 10MHz
- 84 LCC/PGA Package
- Advanced 2-micron CMOS Process

APPLICATIONS

- Digital Signal Processing
- Digital Radio
- Radar Processing
- Sonar Processing
- Robotics

ASSOCIATED PRODUCTS

PDSP16112 16 x 12 Complex Multiplier
PDSP16318 Complex Accumulator
PDSP16116 16 x 16 Complex Multiplier

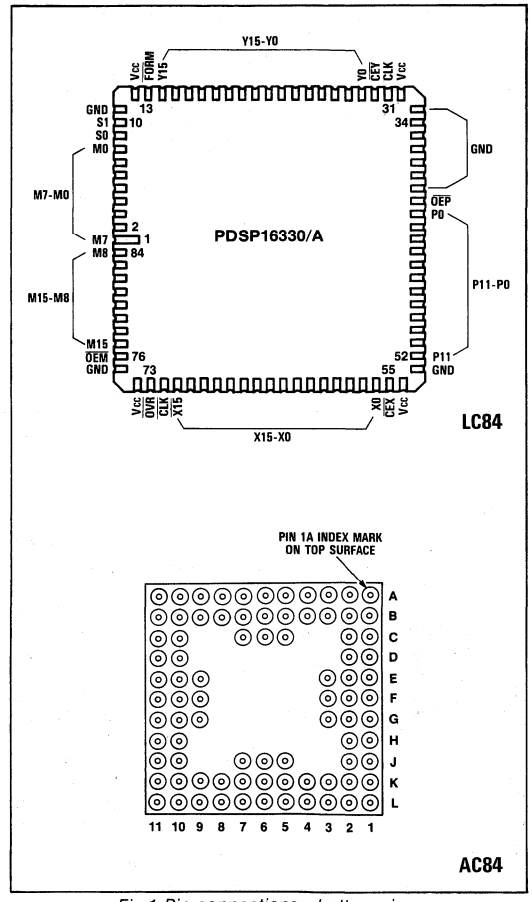


Fig.1 Pin connections - bottom view

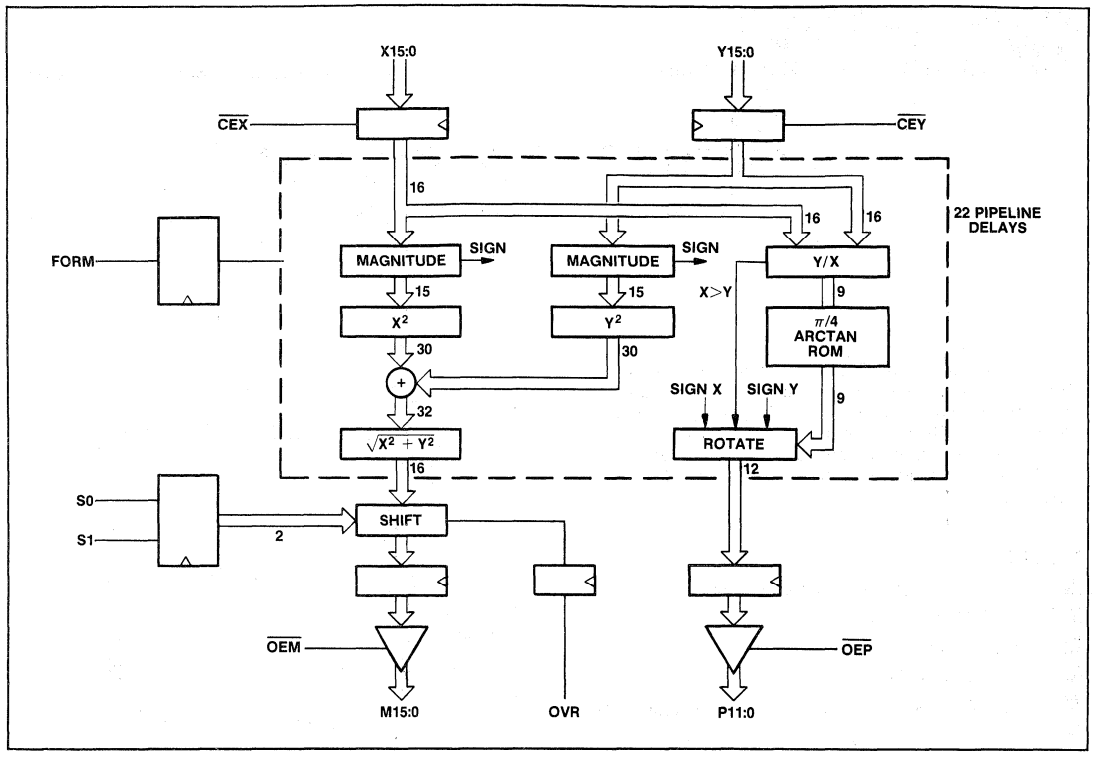


Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16330 converts incoming Cartesian Data into the equivalent Polar Values. The device accepts new 16 +16 bit complex data every cycle, and delivers a 16 bit + 12 bit Polar equivalent after 24 clock cycles.The input data can be in Twos Complement or Sign Magnitude format selected via the FORM input. The output is in a magnitude format for both the Magnitude output and the Phase. Phase data is zero for data with a zero Y input and positive X, and is 400 hex for zero X data and positive Y, is 800 hex for zero Y data and negative X, and is C00 hex for zero X and negative Y. The LSB weighting (bit 0) is 2 x π/4096 radians. The 16 bit Magnitude result may be scaled by shifting one, two, or three places in the more significant direction, effectively multiplying the Magnitude result by 2, 4 or 8 respectively. Any of these shifts can under certain conditions cause an invalid result to be output from the device. Under these circumstances the OVR output will become active. The PDSP16330 has independent clock enables and three state output controls for all ports.

FORM This input selects the format of the X and Y input data. A low level on FORM indicates that the input data is twos complement format (Note: input data 8000 hex is not valid in twos complement mode). This input refers to the format of the current input data, and may be changed on a per cycle basis if desired. The level of FORM is latched at the same time as the data to which it refers.

S1-0 These inputs select the scaling factor to be applied to the Magnitude output. These inputs are latched by the rising edge of CLK, and determine the scaling of the output in the cycle after they are loaded into the device. The scale factor applied is determined by the table. Should the scaling factor applied cause an invalid Magnitude result to be output on the M Port, then the OVR Flag will become active for the period that the M port output is invalid.

S1	S0	Scaling Factor
0	0	x1
0	1	x2
1	0	x4
1	1	x8

The output number range is from 0 to 2 when the scaling factor is set at x1.

PIN DESCRIPTIONS

Symbol	Pin No.*	Pin Name and Description
CLK	31, 72	**Clock:** Common Clock to device Registers. Register contents change on the rising edge of clock. Both pins must be connected.
$\overline{CEX}$	55	**Clock Enable:** Clock Enable for X Port. The clock to the X port is enabled by a low level.
$\overline{CEY}$	30	**Clock Enable:** Clock Enable for Y Port. The clock to the Y port is enabled by a low level.
X15-X0	71-56	**X Data Input:** Data presented to this input is loaded into the device by the rising edge of CLK. X15 is the MSB.
Y15-Y0	14-29	**Y Data Input:** Data presented to this input is loaded into the device by the rising edge of CLK. Y15 is the MSB.
M15-M0	77-84 1-8	**M Data Output:** Magnitude data generated by the device is output on this port. Data changes on the rising edge of CLK, M15 is the MSB. The weighting of M15 is determined by the Scale factor selected.
P11-P0	52-41	**P Data Output:** Phase data generated by the device is output on this port. Data changes on the rising edge of CLK, P11 is the MSB. The weighting of P11 is π radians.
$\overline{OEM}$	76	**Output Enable:** Output Enable for M Port. The M Port is in a high impedance state when this input is high.
$\overline{OEP}$	40	**Output Enable:** Output Enable for P Port. The P Port is in a high impedance state when this input is high.
FORM	13	**Format Select:** This input selects the format of the Cartesian Data input on the X and Y ports. This input is latched by the rising edge of CLK, and is applied at the same time as the data to which it refers. A low level indicates that two's complement data is applied, a high indicates Sign-Magnitude.
S1-S0	10, 9	**Scaling Control:** Control input for scaling of Magnitude Data. This input is latched by the rising edge of CLK, and determines the scaling to be applied to the Magnitude result. The Scaling is applied to the output data in the cycle following the cycle in which the control was latched.
OVR	73	**Overflow:** Overflow flag. This signal becomes active if the scaling currently selected causes an invalid value to be presented to the Magnitude output.
Vcc	12, 32, 54, 74	+ **5V supply.** All Vcc pins must be connected.
GND	11, 33, 34, 35, 36, 37, 38, 39, 53, 75	**0V supply.** All GND pins must be connected.

*Pin numbers are for LC package. For AC package see Pin Function table.

INPUT DATA RANGE

Twos Complement	Sign Magnitude
7FFF	7FFF
.	.
.	.
.	.
0001	0001
0000	{0000 8000}
FFFF	8001
.	.
.	.
.	.
8001	FFFF

PIN FUNCTION

Pin No.		Function	Pin No.		Function	Pin No.		Function
LC	AC		LC	AC		LC	AC	
1	F3	M7	29	L9	Y0	57	A9	X1
2	G3	M6	30	L10	$\overline{CEY}$	58	B8	X2
3	G1	M5	31	K9	CLK	59	A8	X3
4	G2	M4	32	L11	V_{CC}	60	B6	X4
5	F1	M3	33	K10	GND	61	B7	X5
6	H1	M2	34	J10	GND	62	A7	X6
7	H2	M1	35	K11	GND	63	C7	X7
8	J1	M0	36	J11	GND	64	C6	X8
9	K1	S0	37	H10	GND	65	A6	X9
10	J2	S1	38	H11	GND	66	A5	X10
11	L1	GND	39	F10	GND	67	B5	X11
12	K2	V_{CC}	40	G10	$\overline{OEP}$	68	C5	X12
13	K3	FORM	41	G11	P0	69	A4	X13
14	L2	Y15	42	G9	P1	70	B4	X14
15	L3	Y14	43	F9	P2	71	A3	X15
16	K4	Y13	44	F11	P3	72	A2	CLK
17	L4	Y12	45	E11	P4	73	B3	OVR
18	J5	Y11	46	E10	P5	74	A1	V_{CC}
19	K5	Y10	47	E9	P6	75	B2	GND
20	L5	Y9	48	D11	P7	76	C2	$\overline{OEM}$
21	K6	Y8	49	D10	P8	77	B1	M15
22	J6	Y7	50	C11	P9	78	C1	M14
23	J7	Y6	51	B11	P10	79	D2	M13
24	L7	Y5	52	C10	P11	80	D1	M12
25	K7	Y4	53	A11	GND	81	E3	M11
26	L6	Y3	54	B10	V_{CC}	82	E2	M10
27	L8	Y2	55	B9	$\overline{CEX}$	83	E1	M9
28	K8	Y1	56	A10	X0	84	F2	M8

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5 to 7.0V
Input Voltage V_{IN}	-0.9 to V_{CC}+0.9V
Output Voltage V_{OUT}	-0.9 to V_{CC}+0.9V
Clamp diode current per pin I_K (See Note 2)	±18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Military	-55°C to +125°C
Industrial	-40°C to +85°C
Commercial	0°C to +70°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

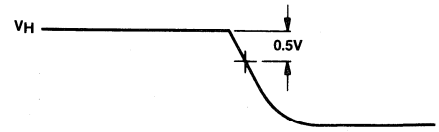
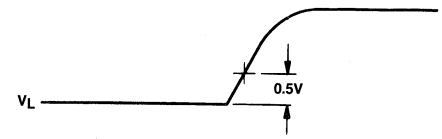
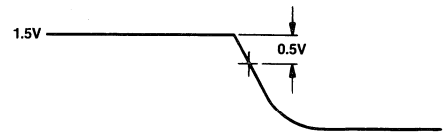
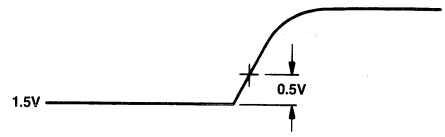
Characteristic	Symbol	Value (Industrial & Military)			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.6	V	I_{OL} = -3.2mA
Input high voltage	V_{IH}	2.2		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current(Note 1)	I_{IL}	-120		+10	μA	GND ≤ V_{IN} ≤ V_{CC}
Input capacitance	C_{IN}	-	10	-	pF	
Output leakage current	I_{OZ}	-10	-	+10	μA	GND ≤ V_{OUT} ≤ V_{CC}
Output S/C current	I_{OS}	24	-	160	mA	V_{CC} = Max.
V_{CC} current	I_{CC}	-	90		mA	10MHz, no load, I/Ps low

NOTES

1. All inputs have high value pull-down resistors.

Switching Characteristics

Characteristic	Value						Units	Conditions
	Industrial		Commercial		Military			
	PDSP16330 B0		PDSP16330A C0		PDSP16330 A0			
	Min.	Max.	Min.	Max.	Min.	Max.		
Input data setup to clock rising edge	15		10		15		ns	
Input data hold after clock rising edge	0		0		0		ns	
FORM, S1-S0 setup to clock rising edge	15		10		15		ns	
FORM, S1-S0 hold after clock rising edge	7			5	7		ns	
Clock rising edge to data valid		40	30			40	ns	2 x LSTTL +20pF
Clock period	100		65		100		ns	
Clock high time	25		20		25		ns	
Clock low time	25		20		25		ns	
Latency	24	24	24	24	24	24	cycles	
$\overline{OEM}$/$\overline{OEP}$ low to output data high valid		30		25		30	ns	2 x LSTTL +20pF
$\overline{OEM}$/$\overline{OEP}$ low to output data low valid		30		25		30	ns	2 x LSTTL +20pF
$\overline{OEM}$/$\overline{OEP}$ high to output data high impedance		30		25		30	ns	2 x LSTTL +20pF
$\overline{CEX}$, $\overline{CEY}$ setup to clock rising edge	30		25		30		ns	
$\overline{CEX}$, $\overline{CEY}$ hold time from clock rising edge	0		0		0		ns	

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to output low	
Delay from output high impedance to output high	

NOTES
1. V_H - Voltage reached when output driven high.
2. V_L - Voltage reached when output driven low.

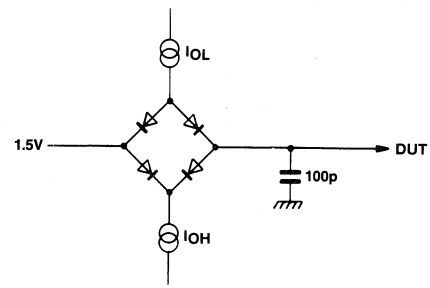


Fig.3 Three state delay measurement load

ORDERING INFORMATION

Industrial (-40 °C to +85 °C)

PDSP16330 B0 LC
PDSP16330 B0 AC

Commercial (0 °C to +70 °C)

PDSP16330A C0 LC
PDSP16330A C0 AC

Military (-55 °C to +125 °C)

PDSP16330 A0 LC
PDSP16330 A0 AC

Call for availability on High Reliability parts and MIL-883C screening.

PDSP16401/PDSP16401A

2-DIMENSIONAL EDGE DETECTOR

(SUPERSEDES APRIL 1987 EDITION)

The PDSP16401 is a single chip CMOS video signal processor which will determine the presence, direction and gradient magnitude of edges in a 3 x 3 pixel frame in a raster scanned image.

FEATURES

- 22 Megapixels/Sec Processing Rate
- 13 Bit Edge Magnitude Output
- 3 Bit Edge Direction Output
- Built-in Threshold Detector
- $P_{tot} < 700mW$ at 22MHz

APPLICATIONS

- Machine Vision
- Image Enhancement
- Pattern Recognition
- Video Effects Generation

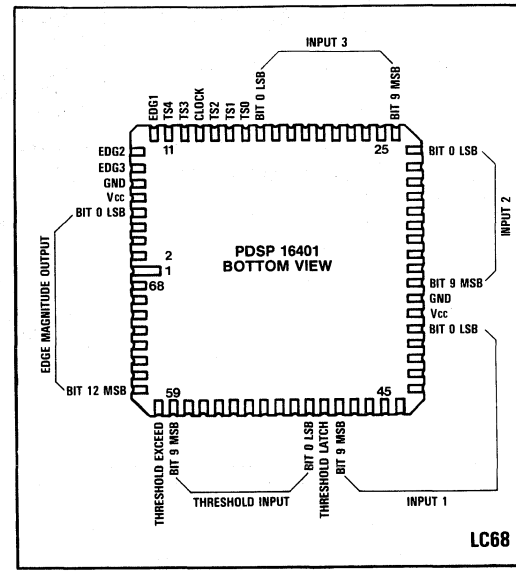


Fig.1 Pin connections - bottom view (not to scale)

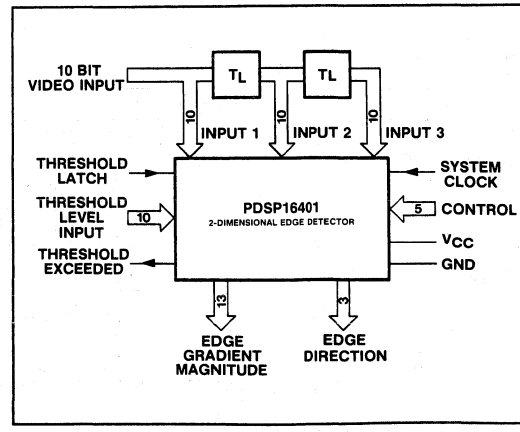


Fig.2 Typical system connection.
The two line stores should have a delay of one line period minus three clock periods.

PIN DESCRIPTION

Pin Nos.	Name	Function
39 to 48	INPUT 1	Input for 10 bits of digitised video corresponding to the current line of the image. Data is unipolar, black level is all zeros. Pin 39 is LSB.
27 to 36	INPUT 2	Input for 10 bits of digitised video corresponding to the previous line of the image (i.e. delayed by 1 line period - 3 x t_{CLOCK}). Data is unipolar, black level is all zeros. Pin 27 is LSB.
17 to 26	INPUT 3	Input for 10 bits of digitised video delayed by (2 line periods) - 6 x t_{CLOCK}. Data is unipolar, black level is all zeros. Pin 17 is LSB.
37, 7	GND	0V supply. Both GND pins must be connected.
38,6	V_{CC}	+5V supply. Both V_{CC} pins must be connected.
49	THRESHOLD LATCH	Used in conjunction with the clock to latch data from THRESHOLD INPUT into DETECTOR input latch. Data is held when THRESHOLD LATCH is low.
50 to 59	THRESHOLD INPUT	10 bits input to THRESHOLD DETECTOR. Data is latched in by THRESHOLD LATCH. Data is compared with 10 MSBs of EDGE MAGNITUDE output. Pin 50 is LSB.
60	THRESHOLD EXCEEDED	Single bit output, logic high when threshold level is exceeded.
5 to 1 & 68 to 61	EDGE MAGNITUDE	13 bits of data representing the largest edge magnitude within the current 3 x 3 pixel image frame. Pin 5 is LSB. Data is in magnitude only format (see Table 2).
10,9,8	EDGE 1-3	3 bits representing the edge direction. See Fig.4 for encoding detail.
13	CLOCK	System clock, no minimum frequency.
11,12,14,15,16	T_{S4} to T_{S0}	Control pins, normally all held low, but can be set to give single filter operation (see Table 2).

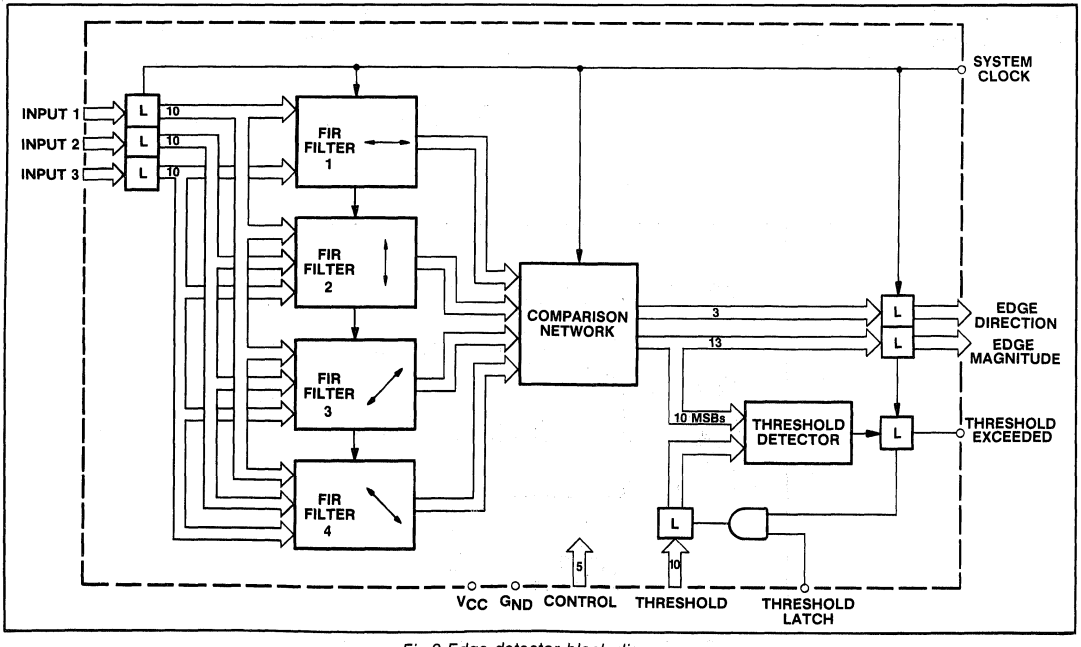


Fig.3 Edge detector block diagram

FUNCTIONAL DESCRIPTION

The PDSP16401 requires three 10-bit wide digitised video inputs, corresponding to three lines of the input image (see Fig.2).

Edges are detected by concurrent convolution of a window consisting of three adjacent pixels in each of the three input lines, with four 3 x 3 masks (Table 1 gives the coefficients of the convolution masks). The four masks are implemented by four separate FIR filters operating in parallel (see Fig.3). Each filter passes video data associated with the orientation of each particular mask. Since within the 3 x 3 window the horizontal or vertical distance between pixels is less than the diagonal distance by a factor of $\sqrt{2}$, the horizontal and vertical mask functions are scaled by a factor of 1.5.

The outputs from the four filters are fed into the comparison network which compares the magnitude of the 13-bit outputs, producing a 3-bit word representing the largest output plus its sign. The sign represents the direction of the edge ie black to white or white to black.

Fig.4 illustrates the coding, where the arrow represents a direction perpendicular to a black-white transition. A 13 bit 2's complement word, which is the magnitude of the output of the filter producing the maximum output is also produced.

The 10 MSBs of the 13-bit magnitude output are internally fed into a threshold detector where they are compared with the external threshold level input. If the output magnitude exceeds the threshold level, the TE output goes high.

ORIENTATION	MASK
HORIZONTAL (Filter 1)	$\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \\ -1 & -1 & -1 \end{bmatrix}$ x 1.5
VERTICAL (Filter 2)	$\begin{bmatrix} 1 & 0 & -1 \\ 1 & 0 & -1 \\ 1 & 0 & -1 \end{bmatrix}$ x 1.5
45° Bottom left to top right (Filter 3)	$\begin{bmatrix} 2 & 1 & 0 \\ 1 & 0 & -1 \\ 0 & -1 & -2 \end{bmatrix}$
45° Top left to bottom right (Filter 4)	$\begin{bmatrix} 0 & -1 & -2 \\ 1 & 0 & -1 \\ 2 & 1 & 0 \end{bmatrix}$

Table 1 Convolutional masks

Control Inputs

Table 2 gives the operations associated with the various control inputs. When a single convolution mask is selected, the edge magnitude comparator is disabled.

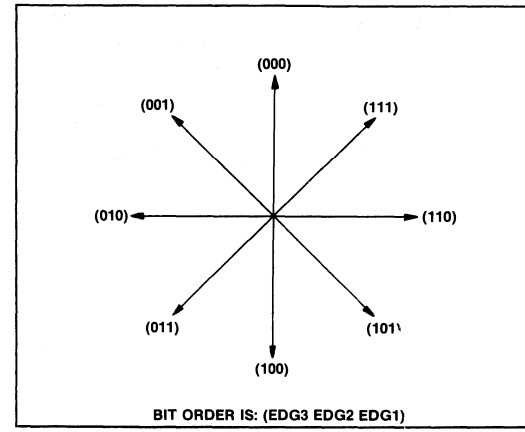
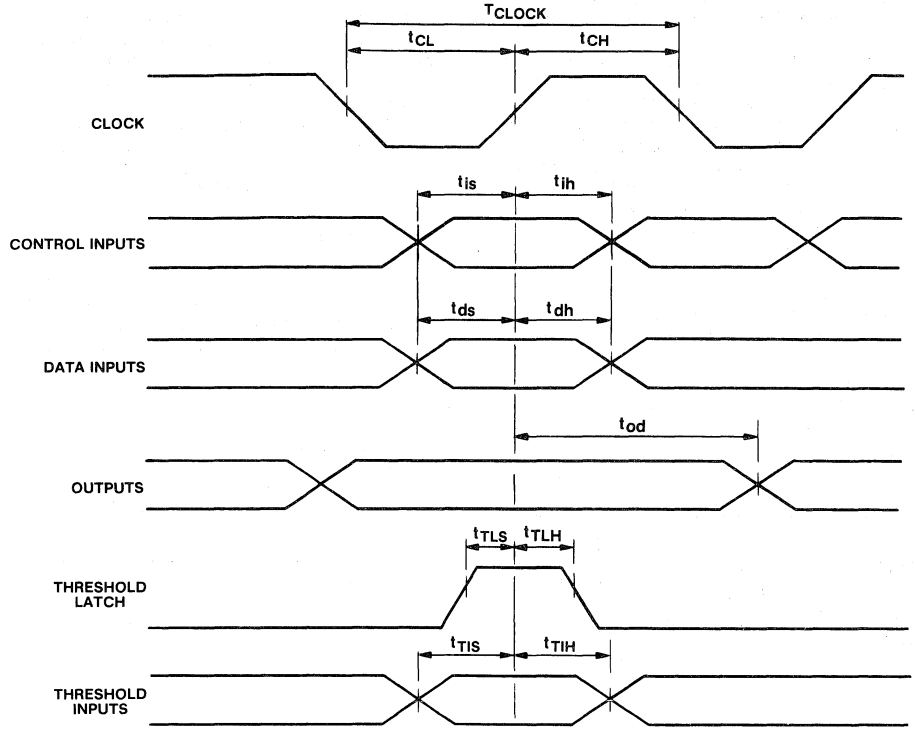


Fig.4 Detail of 3-bit word representation of edge orientation

			Pin Nos. and Codes					Magnitude Output Format
	Package Pin Number		16	15	14	12	11	
	Package Pin Name		TS0	TS1	TS2	TS3	TS4	
Logic Levels	Normal Edge Detection Mode		0	0	0	0	0	Magnitude
	Single* Direction Sensing Mode	Filter 1**	1	1	1	1	0	2's Comp
		Filter 2**	0	0	0	1	0	2's Comp
		Filter 3**	1	0	1	1	0	2's Comp
		Filter 4	0	0	1	1	0	2's Comp

*14th Bit (MSB) appears on EDG3 in Single Filter Mode.
**When using Filters 1, 2 and 3 - all output bits are inverted.

Table 2 Control pin codes and functions



f_{CLOCK}	Clock frequency	t_{TLS}	Threshold latch to clock set-up time
t_{CL}	Clock duration low	t_{TLH}	Threshold latch to clock hold time
$\frac{t_{CL}}{t_{CH}}$	Mark/Space	t_{TIS}	Threshold inputs to clock set-up time
t_{CH}	Clock duration high	t_{TIH}	Threshold inputs to clock hold time
t_{ds}	Input to clock set-up time	t_{ih}	Control input to clock hold time
t_{dh}	Input to clock hold time		
t_{is}	Control input to clock set-up time		
t_{od}	Delay clock to output valid		

Fig.5 Timing diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	±18mA
Static discharge voltage (HMB)	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	7	36

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Industrial) = -40°C to +85°C, V_{CC} = 5.0V ± 10%, GND = 0V

T_{amb} (Military) = -55°C to +125°C, V_{CC} = 5.0V ± 10%, GND = 0V

Static Characteristics

Characteristic	Symbol	Value Ind./Military PDSP16401			Value Ind. Only PDSP16401A			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			2.4			V	I_{OH} = 4mA
Output low voltage	V_{OL}			0.6			0.6	V	I_{OL} = -4mA
Input high voltage	V_{IH}	2.2			2.2			V	
Input low voltage	V_{IL}			0.8			0.8	V	
Input leakage current	I_L	-10		+10	-10		+10	μA	$GND \leq V_{IN} \leq V_{CC}$
Output short circuit current (Note 2)	I_{OS}	12		80	12		80	mA	V_{CC} = max.
Input capacitance	C_I		10			10		pF	

Switching Characteristics

Characteristic	Symbol	Value Industrial PDSP16401			Value Industrial PDSP16401A			Value Military		Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{CC} current	I_{CC}			100			140		100	mA	V_{CC} = max f_{CLK} = max. No O/P loading I/Ps low
CLK frequency	f_{CLK}			15			22		15	MHz	
Min. CLK low		25			20			25		ns	
Min. CLK high		25			20			25		ns	
Input setup time (data)	t_{ds}	30			25			30		ns	
Input hold time (data)	t_{dh}	3			3			3		ns	
Input setup time (control)	t_{is}	50			40			50		ns	
Input hold time (control)	t_{is}	3			3			3		ns	
Delay, clock to output	t_{od}			50			35		50	ns	
Threshold latch to clock setup time	t_{TLS}	10			5			10			
Threshold latch to clock hold time	t_{TLH}	3			3			3		ns	
Threshold input to clock setup time	t_{TIS}	15			10			15		ns	
Threshold input to clock hold time	t_{TIH}	3			3			3		ns	
Latency, input to edge magnitude output		20		20	20		20	20		cycles	
Latency, threshold input to threshold exceeded		3		3	3		3	3		cycles	

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16401 B0 LC (Industrial - LCC package)
PDSP16401A B0 LC (Industrial - LCC package)

Military (-55°C to +125°C)

PDSP16401 A0 LC (Military - LCC package)

Call for availability on High Reliability parts and MIL-883C screening.

Application Notes

A 50ns BUTTERFLY PROCESSOR

Plessey Semiconductors PDSP16112A Complex Multiplier and PDSP16318A Complex Accumulator have been designed to allow the calculation of Radix 2 Decimation in Time Butterfly operations at very high speeds. One PDSP16112A in conjunction with two PDSP16318As is capable of generating a new result every 50ns whilst dissipating less than 1.5W, giving a 1024 point complex Fast Fourier Transform in just 256µs - almost an order of magnitude faster than the current norm.

Fig 1 shows the Butterfly operation diagrammatically, each Butterfly operation requires one Complex Multiplication, one Complex addition and one Complex subtraction.

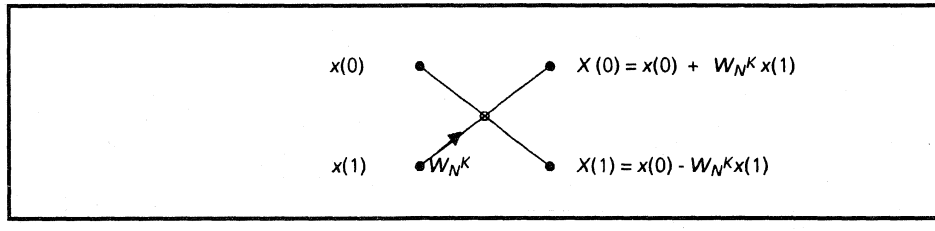


Fig 1 The Butterfly

Figure 2 shows how the devices are connected to form a hardware Butterfly Processor. The PDSP16112A Complex Multiplier calculates $x(1)W_N^K$, the two PDSP16318As calculate respectively the real and imaginary parts of $x(0) + x(1)W_N^K$ and $x(0) - x(1)W_N^K$. The data format employed is fractional 2's complement, the data entering the PDSP16318s has had the binary point shifted right one place since the number range of the 17 bit output, P, from the PDSP16112 is $-2 \leq P < 2$. Three shift control lines allow control of the overall scaling factor, output overflow is indicated by the OVR flag which is active if the MSB goes above bit 15 of the output.

The PDSP16318s contain delay registers which compensate for the pipeline delay through the PDSP16112 Complex Multiplier in order to simplify addressing. The X(0) and X(1) outputs occur 9 cycles after the corresponding x(0) and x(1) inputs.

Application Note AN47 describes the Butterfly Processor in greater detail, while Application Note AN50 describes a complete FFT Processor built around the 50ns Butterfly Processor.

For those applications where very high speed is required, multiple Butterfly Processors may be used. Ten processors in a pipeline array can execute a 1024 point Complex FFT every 26µs, one Processor handling each column of the transform.

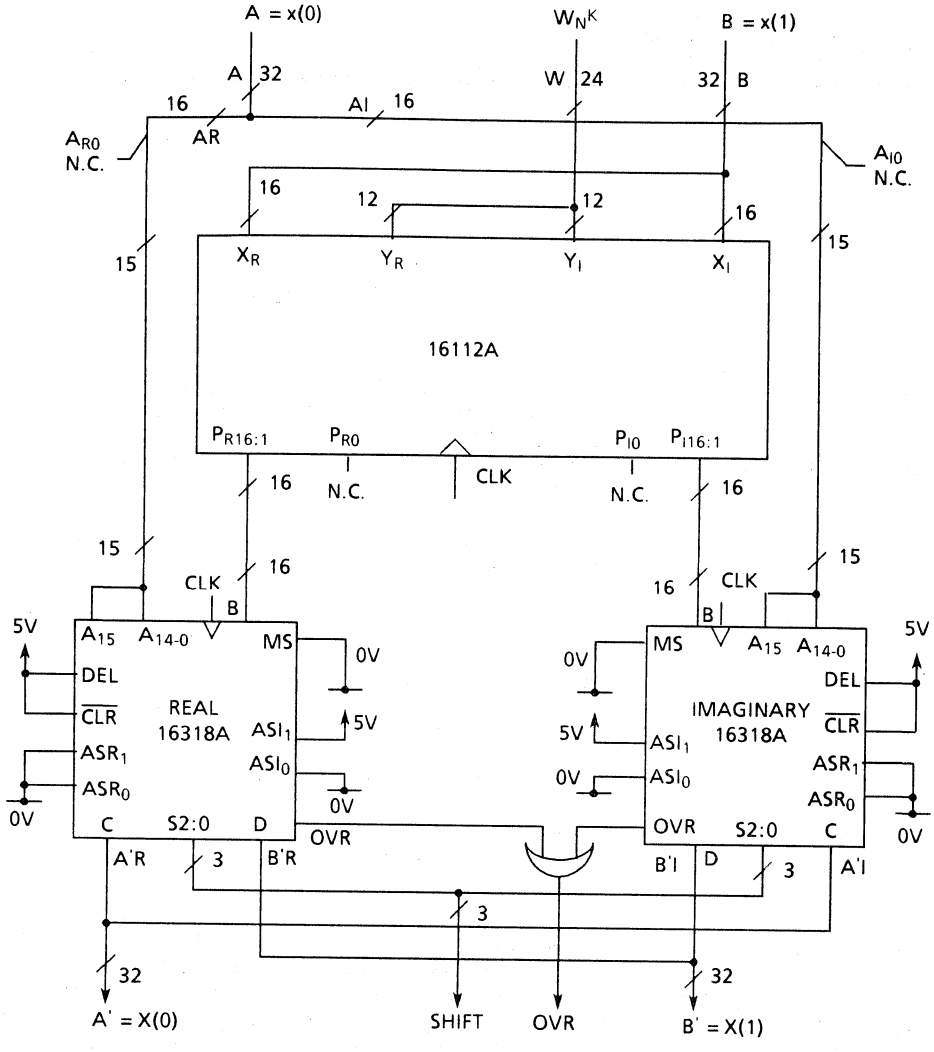

A = x(0)
W_N^K
B = x(1)
A
32
W
24
32
B
16
AR
AI
16
A_{R0}
N.C.
A_{I0}
N.C.
16
12
12
16
15
15
X_R
Y_R
Y_I
X_I
16112A
$P_{R16:1}$
P_{R0}
P_{I0}
$P_{I16:1}$
16
N.C.
CLK
N.C.
16
15
15
CLK
16
16
CLK
5V
A_{15}
A_{14-0}
B
MS
0V
DEL
$\overline{CLR}$
REAL
16318A
ASI_1
5V
ASR_1
ASI_0
ASR_0
0V
C
S2:0
D
0V
OVR
A'R
3
B'R
0V
MS
A_{15}
A_{14-0}
5V
DEL
5V
IMAGINARY
16318A
$\overline{CLR}$
ASI_1
ASR_1
0V
ASI_0
ASR_0
OVR
S2:0
C
0V
B'I
D
3
A'I
3
32
32
A' = X(0)
SHIFT
OVR
B' = X(1)

Fig 2

WAVEFORM SYNTHESIS USING THE PDSP1640/PDSP1640A

The PDSP1640 is a programmable 8-bit address generator capable of operating at a clock speed of up to 40MHz. The device provides a flexible solution to many address generation problems in the field of digital signal processing and is ideally suited to applications using other devices from the Plessey DSP range

Using the PDSP1640 for waveform synthesis takes advantage of a number of device features such as its variable step size, conditional instruction execution and the ability to cascade a number of devices together. By continuously cycling through a sequence of addresses and using these to address a PROM programmed with a particular waveform data pattern, it is possible to generate that waveform as a series of data words appearing at the output of the PROM. Using the PDSP1640 allows that address sequence to be selected and varied as required to produce waveforms of different shape and frequency.

The block diagram of fig 1 shows two PDSP1640 devices cascaded to provide a possible address range of 64K memory locations. By selecting different start and end addresses, different wave shapes may be selected from several possible waveforms held within the PROM. By selecting different incremental step sizes, different subsets of the waveform data may be specified such that some data samples are jumped over at each step, thus varying the generated waveform frequency. Alternatively, if the least significant n address bits are not used to address the PROM, these bits may be considered as a divide by 2^n prescaler for the input clock frequency, which again may be varied by changing the incremental step size.

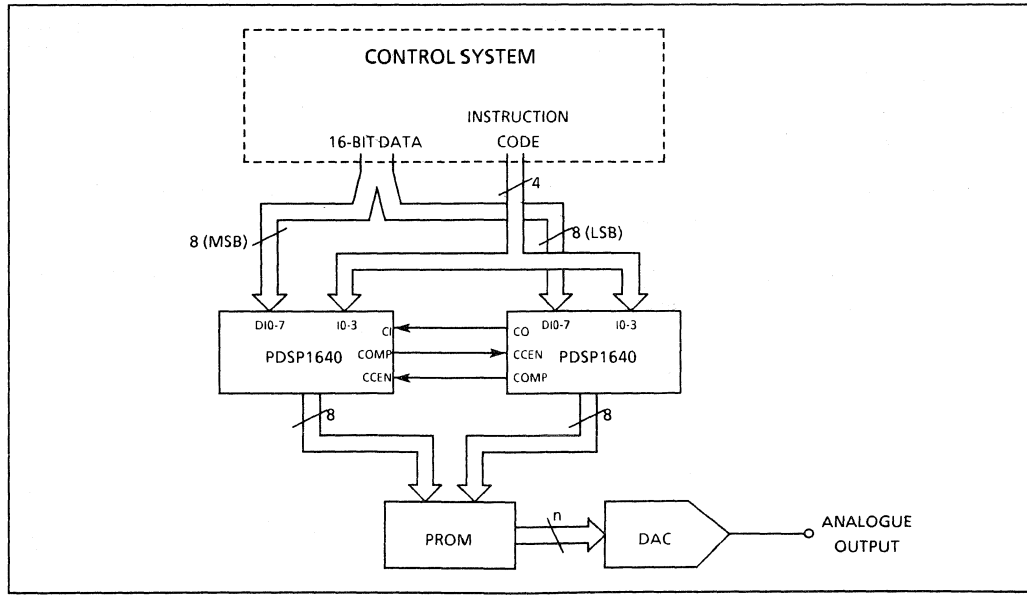


Fig 1 Waveform Generator using PDSP1640s

CYCLE NO.	MNEMONIC	OP. CODE	DATA	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LCRDI	4H	XX	LOAD COUNT REGISTER
3	LIRDI	CH	START ADDRESS	LOAD INCREMENT REGISTER
4	LS1DI	8H	STEP SIZE	LOAD SR1 WITH BRANCH ADDRESS
5	LCPDI	EH	BRANCH ADDRESS	LOAD COMPR WITH STOP ADDRESS
6	CCJS1	1H	STOP ADDRESS	COUNT BY INC OR GO TO SR1
7	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
etc				

Table 1 Waveform Generator Instruction Sequence

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

The required waveform is achieved by using a very simple instruction sequence to program the PDSP1640 and is shown in table 1. The first instruction clears the count register and disables the mask logic. The count register and increment register are then loaded with the start address and step size respectively for the required waveform. The Start 1 register is loaded with the branch address to which a jump is made when the final address for the specified waveform is reached. The branch address will normally be the same as the waveform start address and the end address is specified by the value loaded into the compare register. The final operation programmed into the1640 instructs the device to increment the count register by the value specified in the increment register. This last instruction must be held on the instruction inputs to enable the device to count on every subsequent clock cycle. This instruction also allows a comparison to be made on each cycle between the resulting count register value and the compare register value to detect when the end address has been reached.

The instruction sequence programmed into cascaded devices is the same for each device, however the data associated with each instruction will vary. For two devices, the data may be considered as being sixteen bits wide, thus the various addresses and the step size are presented as sixteen bit numbers, the least significant eight bits to one device and the most significant eight bits to the other. The device which generates the most significant eight bits of the address will normally have a step size of zero, only incrementing by one whenever a carry out from the least significant device occurs.

The eight bit output from the PROM is fed into a fast digital to analogue converter, such as the Plessey MV95408 CMOS DAC, to reconstruct the analogue waveform.

Application Note AN44 describes the use of the Plessey PDSP1640 for waveform generation in greater detail and includes information on a demonstration system.

A 50 ns COMPLEX MULTIPLIER/ACCUMULATOR

The applications of complex multiplier/accumulators include digital demodulation, image rejection mixers, adaptive equalization, digital filtering, discrete Fourier Transforms and convolution. The PDSP16112A and PDSP16318A together form a complex multiplier/accumulator capable of generating a new result every 50ns in a system operating on a 20 MHz clock.

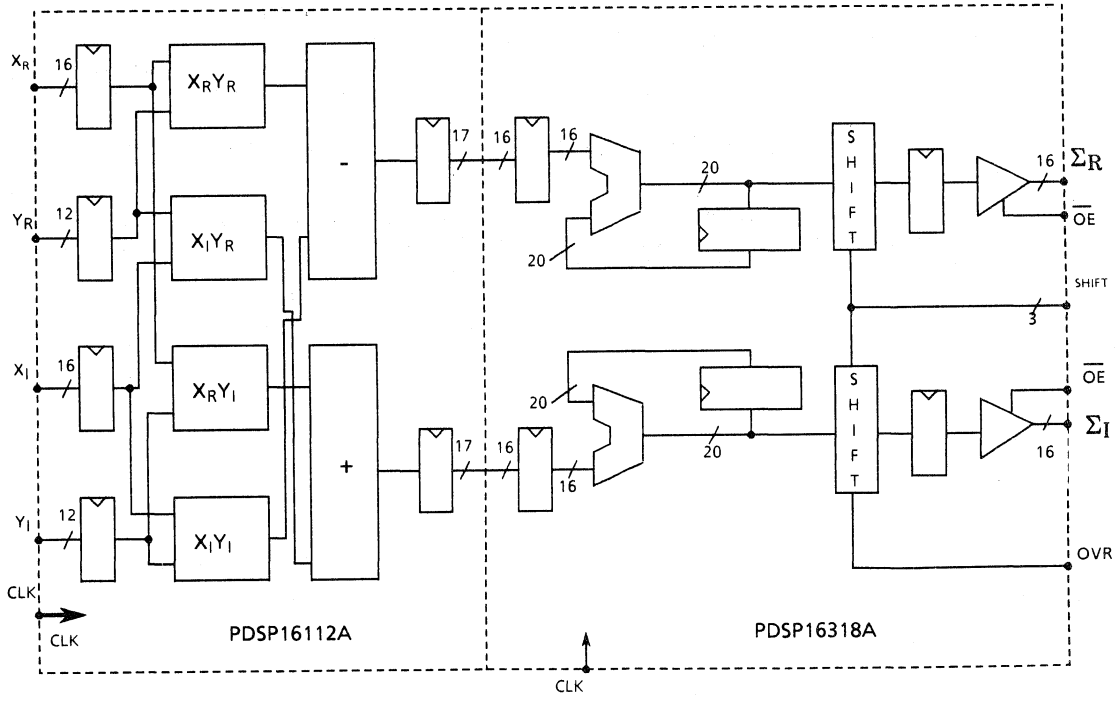


Fig 1

Fig 1 shows the block diagram of the CMAC. The PDSP16112A contains four 16x12 array multipliers, an adder, and a subtractor. The PDSP16318A provides two independent 20-bit-wide add-latch loops for accumulation, followed by output scaling shifters to generate a 16-bit output. If the MSB of the accumulator output goes outside the selected 16-bit output field the overflow flag (OVR) becomes active.

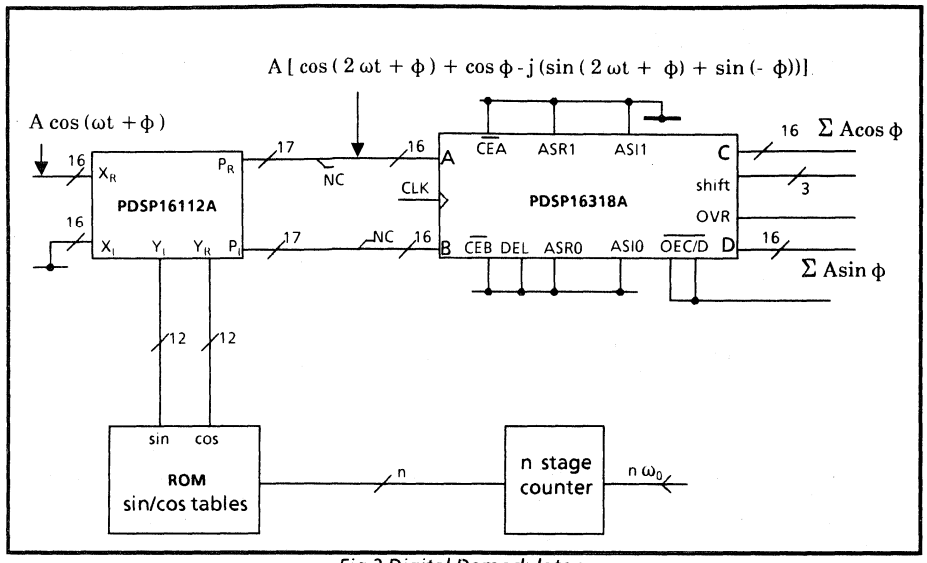


Fig 2 Digital Demodulator

Fig 2 illustrates an application of the complex MAC as a digital demodulator. The input signal A cos (ωt + ϕ) may be phase and/or amplitude modulated with ϕ or A having a finite number of values which are held constant over the symbol period. The input is multiplied by $2e^{-j\omega t}$ (= cos ωt - j sin ωt) to give an output which, when integrated over the signal period in the accumulator, gives an output Σ A cos ϕ + j Σ A sin ϕ from which the original modulation is easily extracted (the PDSP16330 Pythagoras Processor is an obvious choice for this purpose).

For further details on Complex Signal Processing with these devices see Application Note AN49 'Complex Signal Processing with the PDSP16000 Family', Applications Brief AB04 - 'The Pythagoras Processor', and Application Brief AB10 'FIR Filtering with the PDSP16112 and PDSP16318'.

THE PYTHAGORAS PROCESSOR

In a signal processing system it is frequently necessary to calculate the modulus and argument of Complex numbers. This operation is particularly common after Fast Fourier Transforms or in coherent receiver systems. The evaluation of $\sqrt{(x^2 + y^2)}$ and arctan (y/x) are far from easy, so approximations are often used. A common technique for estimating the magnitude of x + jy is to take the larger value of x or y and add to it half the smaller value. The PDSP16330 Pythagoras Processor is a dedicated DSP engine capable of accurate calculation of both magnitude (modulus) and phase (argument) of Complex data at a rate of 100ns per sample.

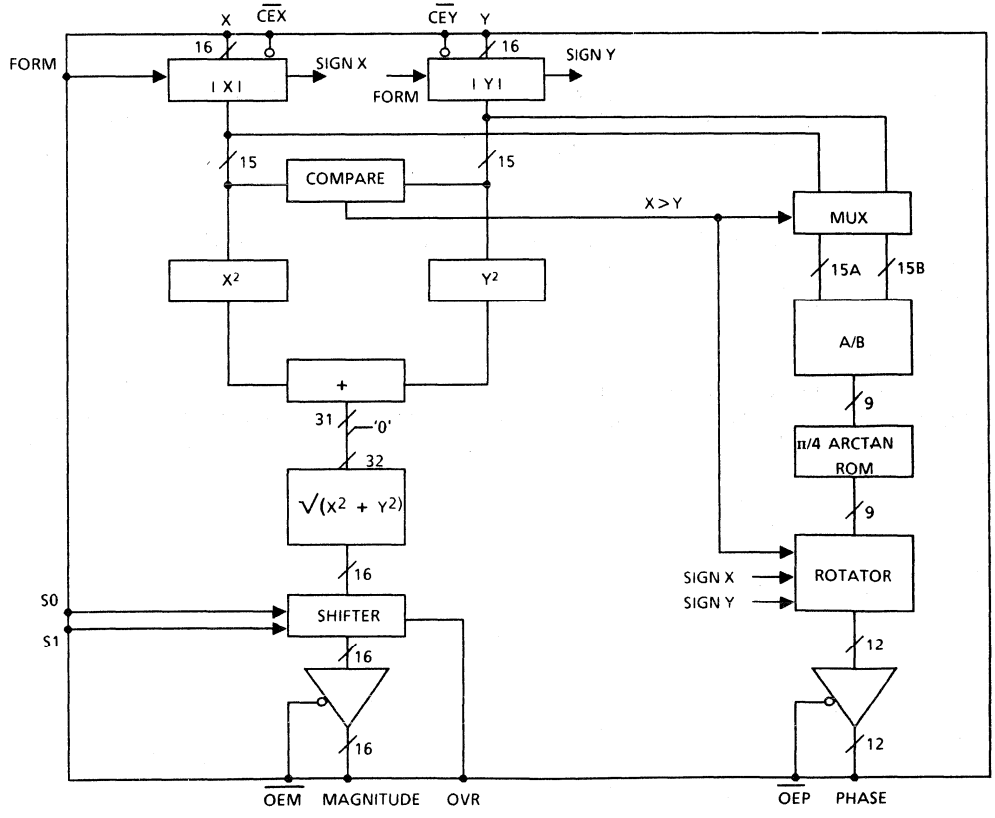


Fig 1 PDSP16330 Block Diagram

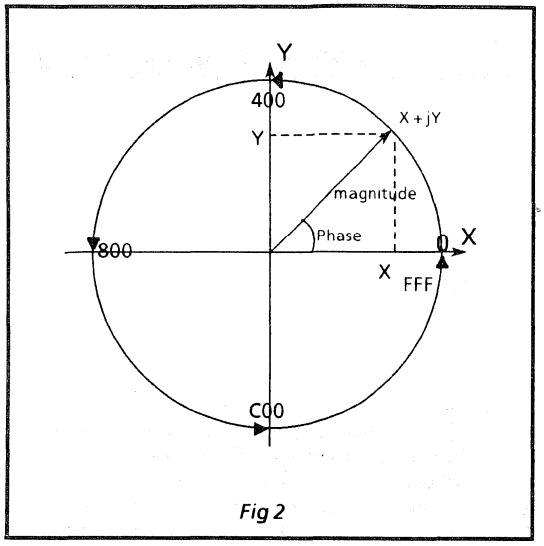


Fig 2

Fig 1 is the block diagram of the device, showing the separate paths for the root sum of squares and arctan (y/x). Fig 2 shows the relationship between the complex input x + jy and the magnitude and phase outputs. Input data can be either 2's complement or sign/magnitude format, depending on the state of the FORM control line.

The magnitude output has a range from 0 to FFFF, four degrees of magnitude output scaling are available via the shift control lines S0 and S1. If the MSB is shifted out of the 0 to FFFF range the OVR flag becomes active, indicating an invalid output. The range of the phase output is 0 to FFF representing a full 2π radians.

APPLICATIONS

FFT.

After an FFT has been carried out the resulting data is complex. This complex data contains information on the magnitude and phase of individual spectral components, but a Cartesian to Polar co-ordinate transformation is required to extract the desired information.

DEMODULATION

In coherent receiver systems the output from the IF stage will have two orthogonal components, I and Q. The carrier may be amplitude or phase modulated, or both. The Pythagoras Processor is used to extract the modulations from the I/Q data.

ROBOTICS

There are many requirements in robotics, position control and position monitoring where conversion from Cartesian space (X,Y, co-ordinates) to polar space (range and angular position) is needed. The Pythagoras Processor is capable of these transformations at very high speeds making it suitable for use even in fast moving machines.

FIR FILTERING WITH THE PDSP16112 AND PDSP16318

The Plessey PDSP16112 Complex Multiplier and PDSP16318 Complex Accumulator are designed to perform very fast calculations on complex digital data for many signal processing applications and as such are ideally suited to the area of digital filtering. Digital filters fall into two groups, those with infinite impulse response (IIR) and those with finite impulse response (FIR). The main difference between these two types is that the output from an FIR filter may be calculated from only current and previous inputs, whereas the output from an IIR filter depends on previous output states as well. Although IIR filters may be designed to be more efficient than an FIR for a given order of filter, consideration must always be given to the stability of any design. FIR filters, on the other hand, are inherently stable, are generally easier to design and implement in hardware and have the additional advantage that they may be designed such that they are free of phase distortion (i.e. constant group delay).

The output, y_n, of an FIR may be calculated as the convolution of the input samples with the filter impulse response and can be represented by a difference equation such as:

$$y_n = b_0 x_n + b_1 x_{n-1} + \ldots\ldots + b_{N-1} x_{n-N+1}$$

or more generally:

$$y(n) = \sum_{k=0}^{N-1} h(k).x(n-k)$$

where coefficients b_k represent the N samples of the impulse response, $h(k)$, of the desired filter.

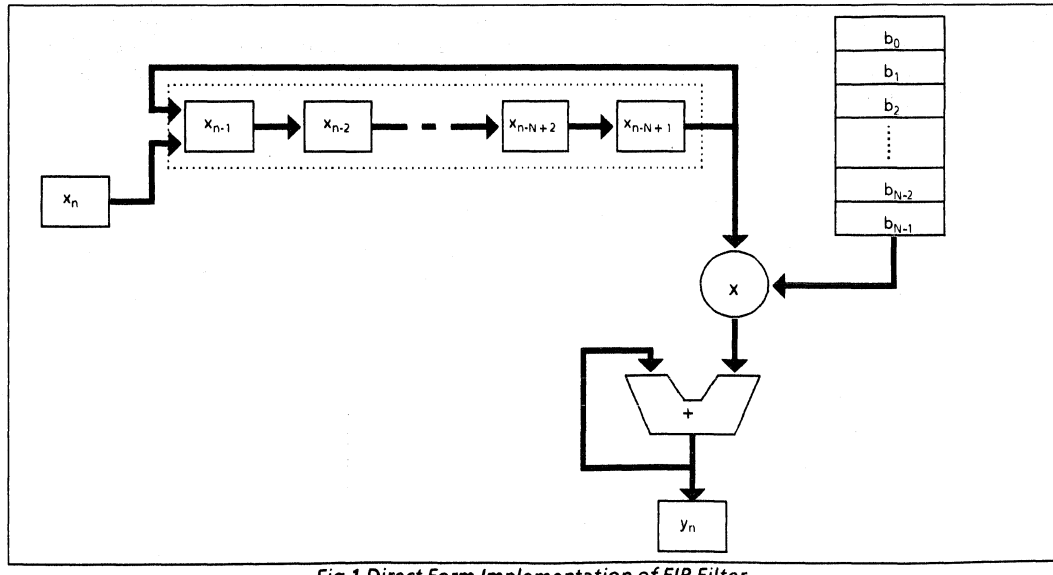


Fig 1 Direct Form Implementation of FIR Filter

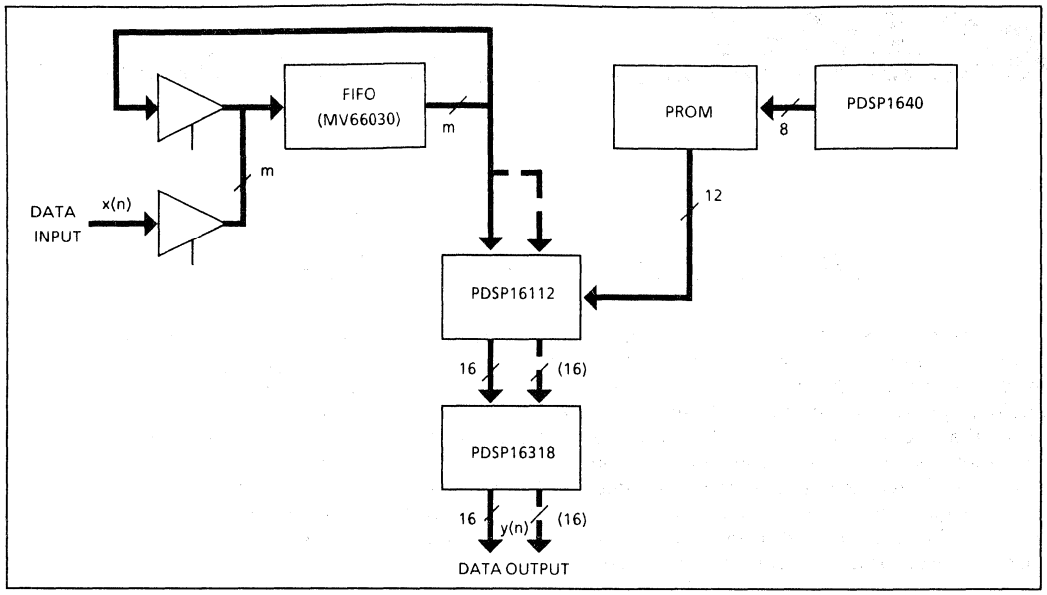


Fig 2 FIR Filter Block Diagram using PDSP16112/16318

An FIR filter may be implemented in a number of ways, but the simplest, with regard to hardware, is termed the direct form, as shown in fig 1. This consists of just one multiplier and one accumulator plus memory to hold the input data and filter coefficients. The data memory is in the form of a shift register or FIFO, whereas the coefficients may reside in PROM. At each new sample, the data is rotated through the shift register, with the newest sample replacing the oldest within the data store. As each sample is rotated around the registers, it is multiplied by its relevant filter coefficient and the total sum accumulated to calculate the new output value.

The PDSP16112 and PDSP16318 allow filtering of either real or complex data at very high speed, being capable of accumulating a new multiplier result every 50ns. This, for example, enables a very simple 128 tap FIR filter to be implemented with an input signal bandwidth of 78kHz. A block diagram of the circuit for an FIR filter using the PDSP16112 and PDSP16318 is shown in fig 2. This circuit also shows the use of a FIFO, such as the Plessey MV66030, as the data store, which may be cascaded to produce the depth and width of registers required, and the PDSP1640 Address Generator to provide the correct address sequence for the coefficient PROM.

INTERFACING THE PDSP FAMILY

INTRODUCTION

Plessey Semiconductors PDSP family of DSP functional blocks are fabricated on a high speed CMOS process, and incorporate several design features to ease interfacing and board layout. However there are a few precautions which should be taken which will ensure trouble-free board design and operation.

All parts in the PDSP family are designed with the generic structure of Fig 1

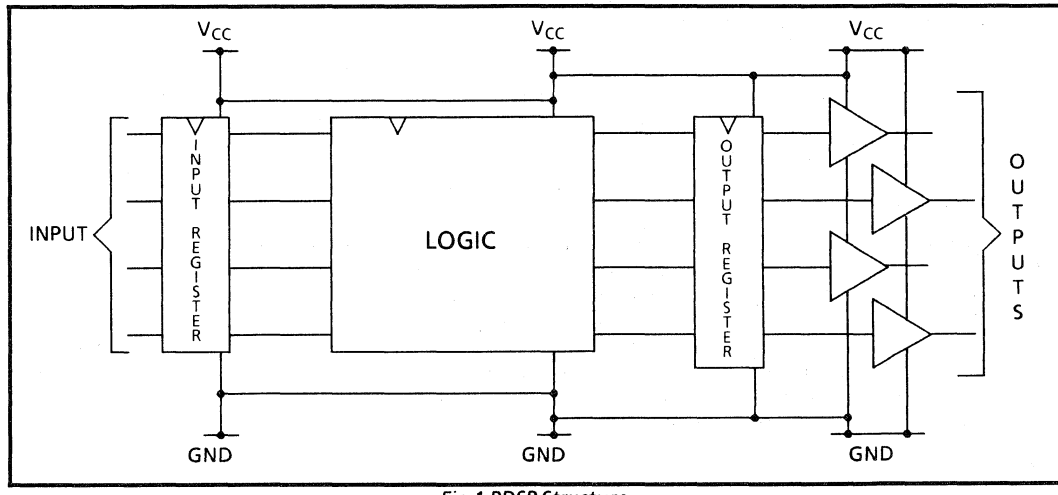


Fig 1 PDSP Structure

The registered input is designed with a positive set-up time (ie data must be presented before the rising edge of the clock) and zero hold time (ie the data is allowed to change anytime after the rising edge of the clock). The input levels are designed for compatability with LSTTL outputs (V_{IH} = 2.2V, V_{IL} = 0.8 V), and the output, although conventional CMOS stages, are specified into a load of 2 standard LSTTL inputs + 20pF for track loading.

All PDSP devices (with the exception of the PDSP16112/A) have tri-state output buffers preceded by an output register, this ensures that the output data is valid for a whole clock cycle. To simplify timing requirements further, the clock to output valid delay is generally less than half a cycle at the maximum specified clock rate.

NOISE

The operating margins of all devices on a board of high-speed logic can best be maintained by providing a quiet environment free of noise spikes, undershoot, and ringing. The key elements in creating such an environment are good supply decoupling and termination of interconnections.

POWER DISTRIBUTION

To maintain wide operating margins across all devices on a board, the supply impedance at each device must be kept to a minimum. The internal design of PDSP devices is such that the input registers, main logic, and output buffers have separate supply pins. This arrangement is designed to ensure that current spikes generated in the output drivers do not modulate the supply to the input gates, hence altering the thresholds. Although these multiple supply pins are internally connected, the internal paths are not particularly low impedance, and therefore each individual V_{CC} pin should be separately decoupled.

The total supply impedance at a device is a function of the supply line impedance and the decoupling capacitors. In practice, the effect of local decoupling does not extend very far, because of the very fast edges of the current spikes generated by CMOS output stages and the inductive nature of the P.C.B. tracks. In order to minimise the effects of these transients, the decoupling capacitors should be high quality, low inductance parts mounted as close as possible to the device pins, with as short a track length as is practical. Capacitor values should be in the 0.1 to 0.47µF region, too small and there will be insufficient decoupling, too large and the equivalent inductance will reduce decoupling efficiency. The quality of the ground connection is also important, this should be either a solid plane or a grid to minimise inductance and prevent loss of noise margin due to differential ground noise between devices.

Low frequency current transients can best be handled by tantalum capacitors mounted close to the edge connector where the panel tracks meet the backplane power distribution system. Such large capacitors provide bulk energy storage which prevents voltage drops due to the long inductive path between the logic board and the system power supply.

TRACK TERMINATION

On a large board P.C.B.tracks look like shorted transmission lines to the signals they are carrying . This causes reflection of the signal resulting in undershoot, overshoot or ringing. Particular cases which can cause difficulty are large RAM arrays being addressed by 1601s or1640s - the long track lengths and heavy capacitative loading can store and reflect amounts of energy leading to severe ringing - and LSTTL to CMOS interface via long tracks which can suffer severe undershoot. In both cases track termination is best effected by a series resistor at the driving end (typically 10 or18ohms). Parallel termination is not recommended since it reduces the voltage swing at the input (making the noise margin even worse), consumes DC power (hardly desirable in a CMOS system) and doesn't work very well in any case.

VERIFICATION

When a board design is complete and the prototype built, it is good practice to check the power supplies to each device and the signals on the busses with a wideband 'scope to ensure that excessive noise, ringing or undershoot isn't present. A board which works on the bench but which is marginal because of noise problems will almost certainly exhibit gremlins in the field.

THREE DIMENSIONAL COORDINATE TRANSFORMS WITH THE PDSP16330

The PDSP16330 is designed to carry out the coordinate transform x,y, → r,θ. many applications in robotics and target positioning require three dimensional transformations of the form x,y,z → r,θ,ø. This application brief shows how the Pythagoras Processor PDSP16330 can be used for three dimensional transforms.

Figure 1 shows a point x,y,z in a three dimensional space. If we move down the z-axis to the point x,y,0, we are at a point whose distance from the origin is $h = \sqrt{(x^2 + y^2)}$ whose bearing is arctan (y/x). The distance from the origin to the point x,y,z is therefore given by $r = \sqrt{(h^2 + z^2)}$ and the elevation of that point given by arctan (z/h). In this way the three dimensional transform x,y,z, → r,θ,ø has been decomposed into two 2-dimensional transforms which can be carried out by the Pythagoras Processor.

Figure 2 shows the most obvious implementation of a 3-D transform, using two Pythagoras Processors. The first processor is given x,y as its input, providing the bearing and the distance to the point x,y,0. The second processor has z (suitably delayed to match the pipeline delay through the first processor) and h as its inputs giving r and ø as its outputs. Output θ from the first processor is delayed so that all three outputs suffer the same pipeline delay.

Figure 3 shows an alternative realisation employing a single Pythagoras Processor. In this case x and y data are input on every other cycle, the alternate cycle inputs being z and h. The z input has a pipeline delay to compensate for the delay on h relative to x and y. This configuration will achieve a throughput of 5MHz, half that of the previous circuit.

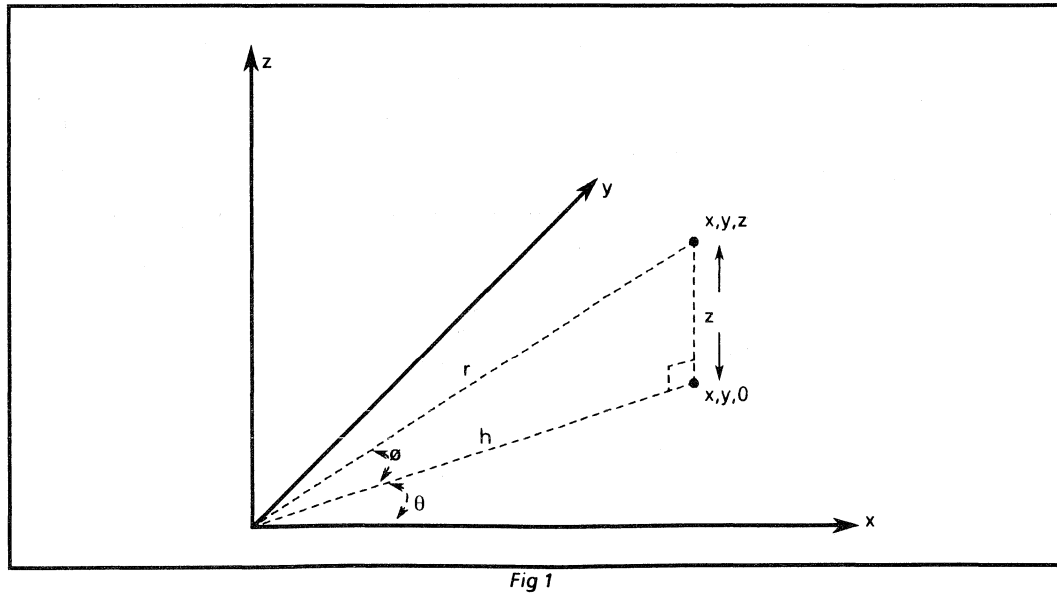


Fig 1

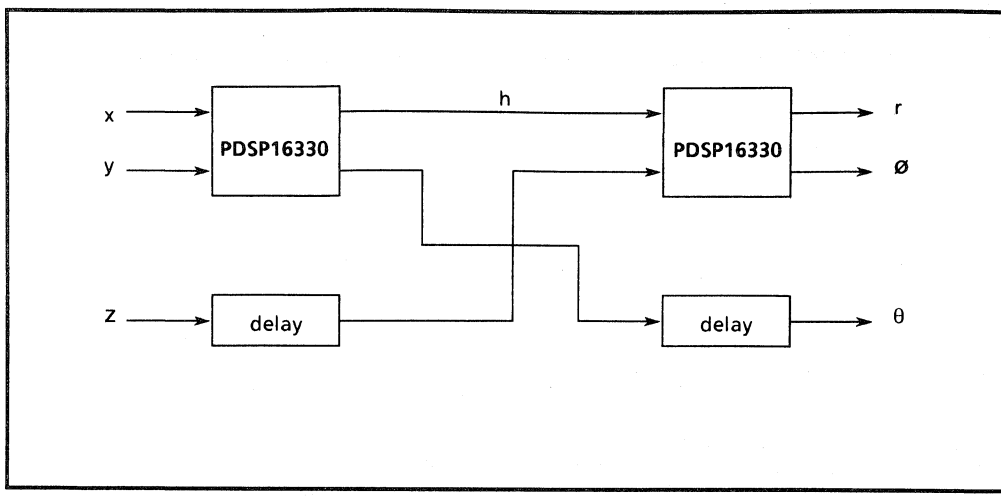

x
y
PDSP16330
h
PDSP16330
r
ø
z
delay
delay
θ

Fig 2

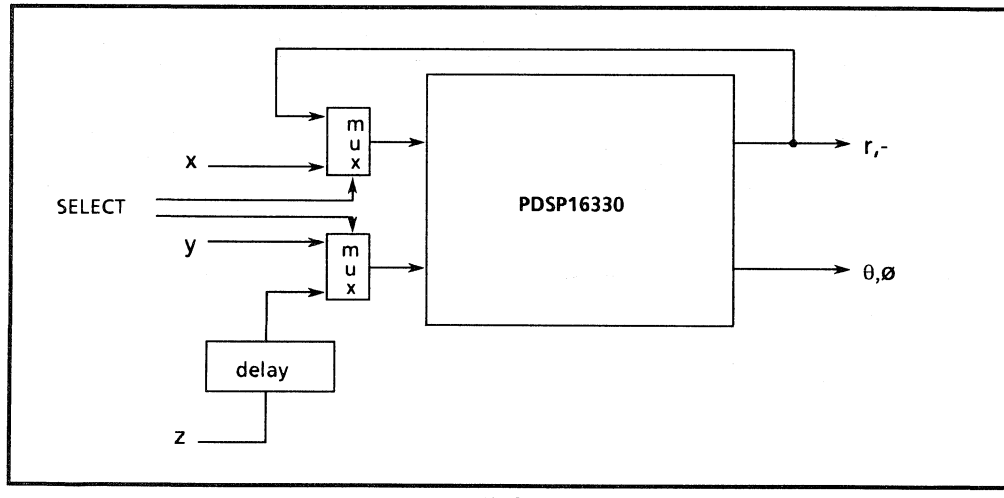

m
u
x
x
SELECT
y
m
u
x
PDSP16330
r,-
θ,ø
delay
z

Fig 3

PDSP1640/PDSP1640A WAVEFORM SYNTHESISER

The PDSP1640 is a programmable 8-bit address generator capable of operating at a clock speed of up to 40MHz. The device provides a flexible solution to many address generation problems in the field of digital signal processing and is ideally suited to applications using other devices from the Plessey DSP range

This application note describes a novel use for the device which takes advantage of a number of device features such as its variable step size, conditional instruction execution and the ability to cascade a number of devices together. By continuously cycling through a sequence of addresses and using these to address a PROM programmed with a particular waveform data pattern, it is possible to generate that waveform. Using the PDSP1640 allows that address sequence to be selected and varied as required to produce waveforms of different shape and frequency.

The block diagram of fig 1 shows two PDSP1640 devices cascaded to provide a possible address range of 64K memory locations. By selecting different start and end addresses, different wave shapes may be selected from several possible waveforms held within the PROM. By selecting different incremental step sizes, different subsets of the waveform data may be specified to vary the generated waveform frequency, as shown in fig 2. Alternatively, if the least significant n address bits are not used to address the PROM, these bits may be considered as a divide by 2^n prescaler for the input clock frequency, which again may be varied by changing the incremental step size (fig 3).

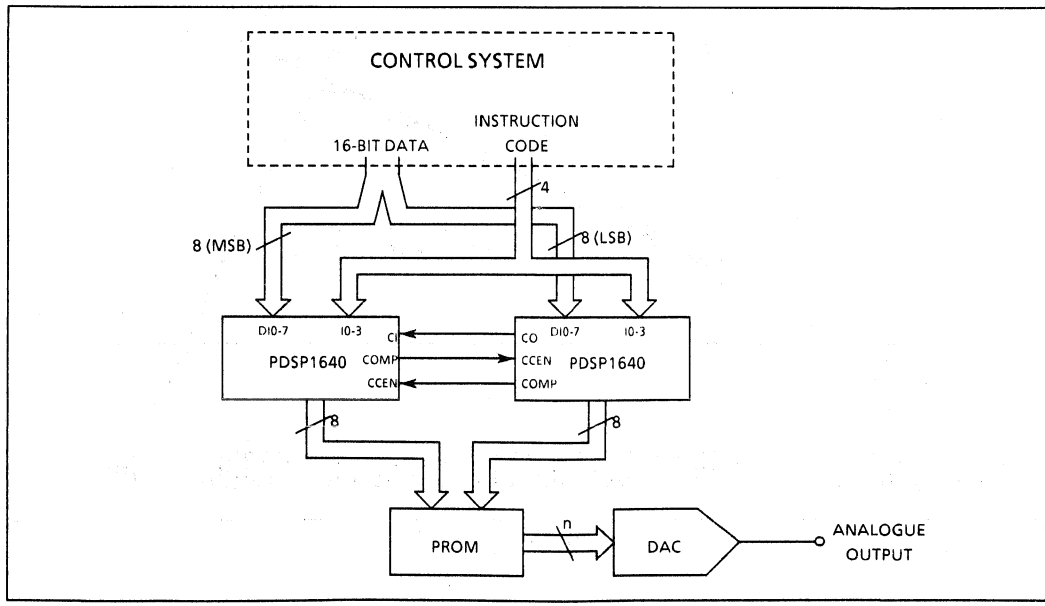


Fig 1 Waveform Generator using PDSP1640s

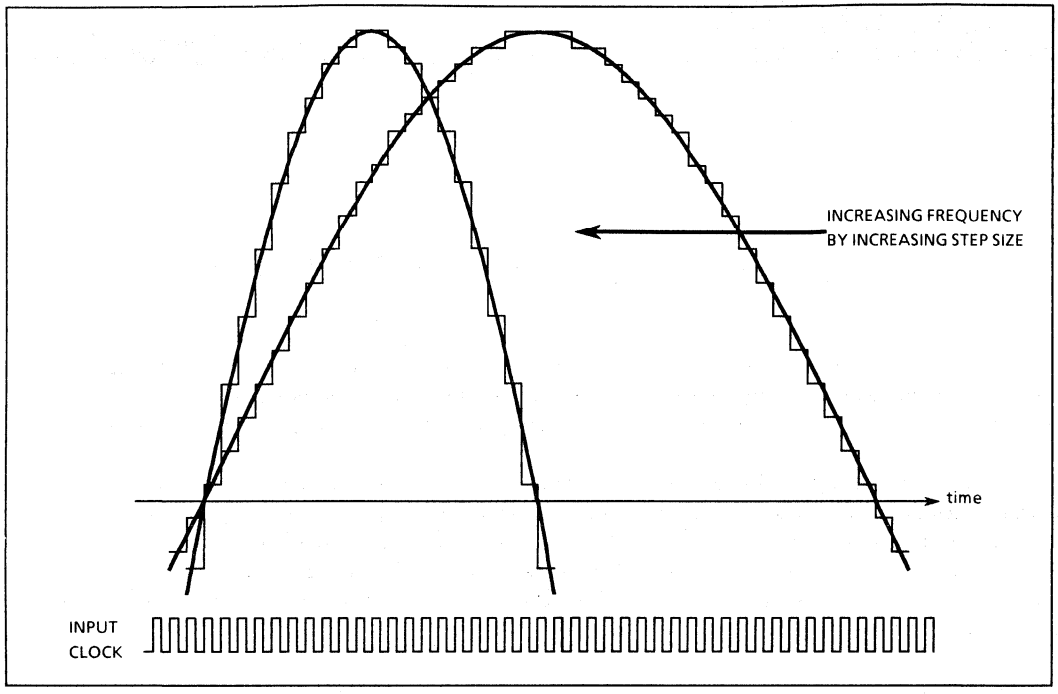


Fig 2 Selecting Subset of Possible Addresses

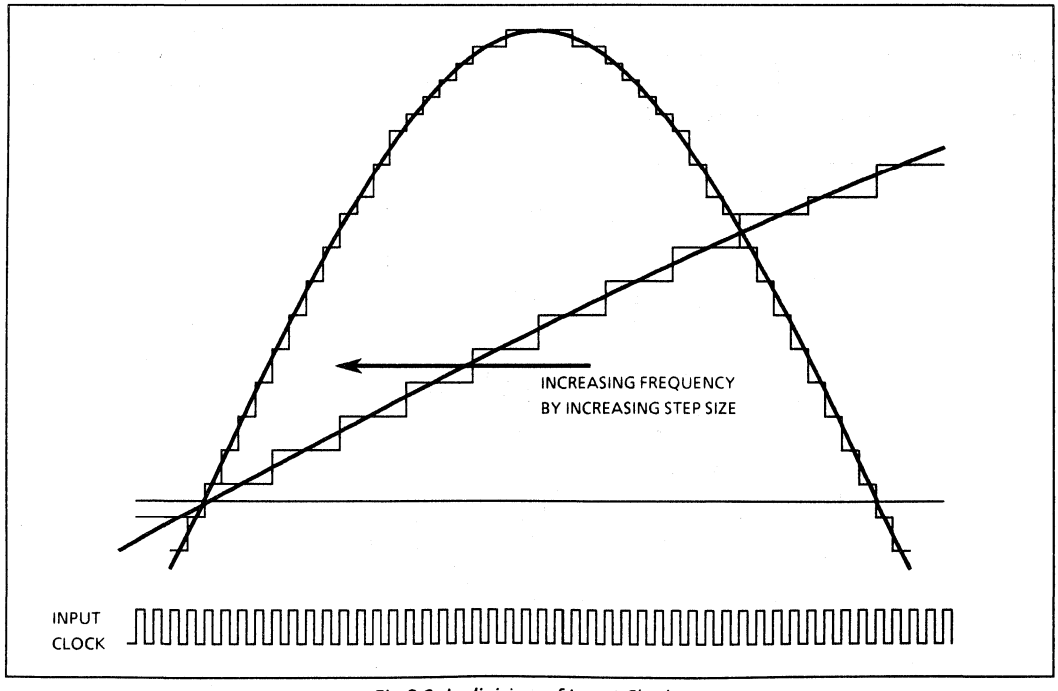


Fig 3 Sub-division of Input Clock

CYCLE NO.	MNEMONIC	OP. CODE	DATA	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LCRDI	4H	XX	LOAD COUNT REGISTER
3	LIRDI	CH	START ADDRESS	LOAD INCREMENT REGISTER
4	LS1DI	8H	STEP SIZE	LOAD SR1 WITH BRANCH ADDRESS
5	LCPDI	EH	BRANCH ADDRESS	LOAD COMPR WITH STOP ADDRESS
6	CCJS1	1H	STOP ADDRESS	COUNT BY INC OR GO TO SR1
7	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
etc				

Table 1 Waveform Generator Instruction Sequence

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

The required waveform is achieved by using a very simple instruction sequence to program the PDSP1640 and is shown in table 1. The first instruction clears the count register and disables the mask logic. The count register and increment register are then loaded with the start address and step size respectively for the required waveform. The Start 1 register is loaded with the branch address to which a jump is made when the final address for the specified waveform is reached. The branch address will normally be the same as the waveform start address and the end address is specified by the value loaded into the compare register. The final operation programmed into the1640 instructs the device to increment the count register by the value specified in the increment register. This last instruction must be held on the instruction inputs to enable the device to count on every subsequent clock cycle. This instruction also allows a comparison to be made on each cycle between the resulting count register value and the compare register value to detect when the end address has been reached.

The instruction sequence programmed into cascaded devices is the same for each device, however the data associated with each instruction will vary. For two devices, the data may be considered as being sixteen bits wide, thus the various addresses and the step size are presented as sixteen bit numbers, the least significant eight bits to one device and the most significant eight bits to the other. The device which generates the most significant eight bits of the address will normally have a step size of zero, only incrementing by one whenever a carry out from the least significant device occurs.

The circuit diagram of fig 4 shows a demonstration system for the PDSP1640 which performs the basic function of the waveform generator described above. Two address generators are used, one to produce an eight bit address for a 256x8 PROM (implemented as two 256x4 PROMs), the other to subdivide the input clock frequency. The PROM contains two waveforms each of 128 points, the appropriate one being selected by switch S2. The operation of this switch alters the start address, end address and branch address loaded into the 1640 which generates the PROM address. This device is programmed to cycle between the addresses of 00H to 7FH or 80H to FFH depending on which waveform is required. The least significant device is programmed to continually cycle through the addresses 00H to FFH, the step size being selected from the 1-of-8 position switch S1, the smallest step size being 1 and each subsequent position being twice the previous one. The step size for the most significant device is set to zero. It is configured to count the number of times the least significant device cycles through its programmed addresses.

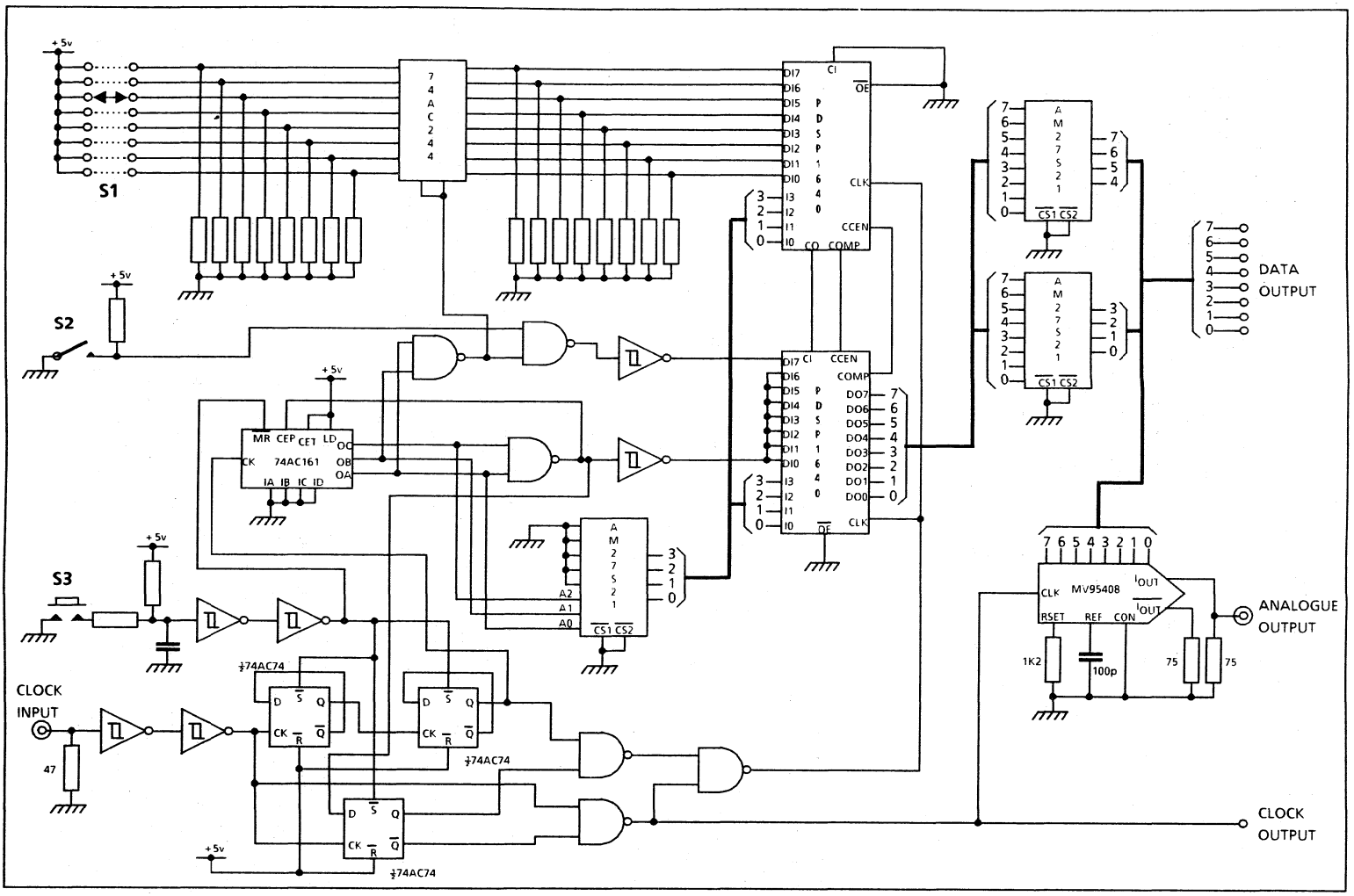


Fig 4 PDSP1640 Waveform Generator Demonstration Circuit Diagram

CYCLE NO.	WAVEFORM 1				WAVEFORM 2			
	MNEMONIC	OP. CODE	DATA MSD	DATA LSD	MNEMONIC	OP. CODE	DATA MSD	DATA LSD
1	CLRCR	7H	XX	XX	CLRCR	7H	XX	XX
2	LCRDI	4H	XX	XX	LCRDI	4H	XX	XX
3	LIRDI	CH	00H	00H	LIRDI	CH	80H	00H
4	LS1DI	8H	00H	NN	LS1DI	8H	00H	NN
5	LCPDI	EH	00H	00H	LCPDI	EH	80H	00H
6	CCJS1	1H	7FH	00H	CCJS1	1H	FFH	00H
7	CCJS1	1H	XX	XX	CCJS1	1H	XX	XX
etc								

Table 2 Waveform Generator Demonstrator Instruction Sequence

Notes-

1. XX = don't care

2. NN = step size from switch S1

3. LSD = least significant device

4. MSD = most significant device

When push-button S3 is pressed and released, the clock input to the address generators is temporarily inhibited whilst the programming cycle is carried out. Six instructions are clocked into the two devices from a 4-bit wide PROM, together with their associated data to select the required waveform address sequence. Table 2 shows the data used to select the desired waveform. Increasing the step size to the least significant device, decreases the value by which the clock frequency is divided, thus increasing the waveform frequency (see fig 3).

The eight bit output from the PROM is fed into a fast digital to analogue converter, such as the Plessey MV95408 CMOS DAC, to reconstruct the analogue waveform.

A RADIX 2 BUTTERFLY PROCESSOR

1.1 INTRODUCTION

The Fast Fourier Transform is a set of algorithms providing short - cuts for the computation of a Discrete Fourier Transform (DFT). FFT techniques can result in calculation times a factor of 100 or more shorter than direct DFTs.

The commonest algorithm used for FFT is the Radix 2 Decimation in Time algorithm, this Application Note illustrates the use of the Plessey PDSP16112 and PDSP16318 in the evaluation of this algorithm.

1.2 THE DFT ALGORITHM

The DFT of a limited sequence of values $\{x(n)\}$, $0 \leq n \leq (N-1)$ is defined as:-

$$X(K) = \sum_{n=0}^{(N-1)} x(n) e^{-j(2\pi/N)nK} \quad , K = \{0,1,2,3.....(N-1)\} \qquad 1$$

that is, for N samples of data in the time domain $\{x(n)\}$ we can calculate a sequence of N values representing the signal in the frequency domain $\{X(K)\}$.

The difficulty with this direct evaluation is that $(N-1)^2$ multiplications and $N^2 - N$ additions must be performed. Clearly, large values of N require huge amounts of computation - a 1024 point DFT requires 2,094,081 arithmetic operations on the data.

1.3 THE FFT ALGORITHM

Equation 1 can be re-written as

$$X(K) = \sum_{n=0}^{(N-1)} x(n)\, W_N^{nK}, \quad where W_N = e^{-j2\pi/N} \qquad 2$$

If we split the sequence $\{x(n)\}$ into its even and odd numbered points then:-

$$X(K) = \sum_{\substack{n=0 \\ \text{even only}}}^{(N-1)} x(n) W_N^{nK} + \sum_{\substack{n=0 \\ \text{odd only}}}^{(N-1)} x(n)\, W_N^{nK} \qquad 3$$

or

$$X(K) = \sum_{n=0}^{(N/2-1)} x(2n)\, W_N^{2nK} + \sum_{n=0}^{(N/2-1)} x(2n+1)\, W_N^{(2n+1)K} \qquad 4$$

Now,

$$W_N^2 = [e^{-j(2\pi/N)}]^2 = e^{-j2\pi/(N/2)} = W_{N/2}$$

and $x_{even}(n) = x(2n)$, $x_{odd}(n) = x(2n+1)$

then

$$X(K) = \sum_{n=0}^{(N/2-1)} x_{even}(n) W_{N/2}^{nK} + W_N^K \sum_{n=0}^{(N/2-1)} x_{odd}(n) W_{N/2}^{nK}$$

the original transform has now divided into two separate smaller transforms combined in the following way:

$$X(K) = Xe(K) + W_N^K Xo(K) \qquad 6$$

where $Xe(K)$ and $Xo(K)$ are the N/2 point DFTs of $x_{even}(n)$ and $x_{odd}(n)$ respectively.

Each of the sub transforms of equation 6 can be split into two, each of these shorter DFTs can then be divided in turn, and so on. If the number of points $N = 2^r$ where r is an integer, then this decimation can be continued until only 2 point DFTs remain.

The 2 point DFT $X(K)$, $K = 0,1$ can be evaluated as

$$X(0) = x(0) + x(1)$$
$$X(1) = x(0) - x(1) \qquad 7$$

Note that there are no multiplications involved in a 2 point DFT as the values of $W_{N/2}^K$ for $K = 0,1$ are ± 1. Non trivial multiplications by W_N^K are necessary in combining together the sub-DFTs, see Equation 6. These multipliers are often referred to as ' twiddle factors'.

Figure 1 shows the decomposition of an N point DFT into two N/2 point DFTs and twiddles.

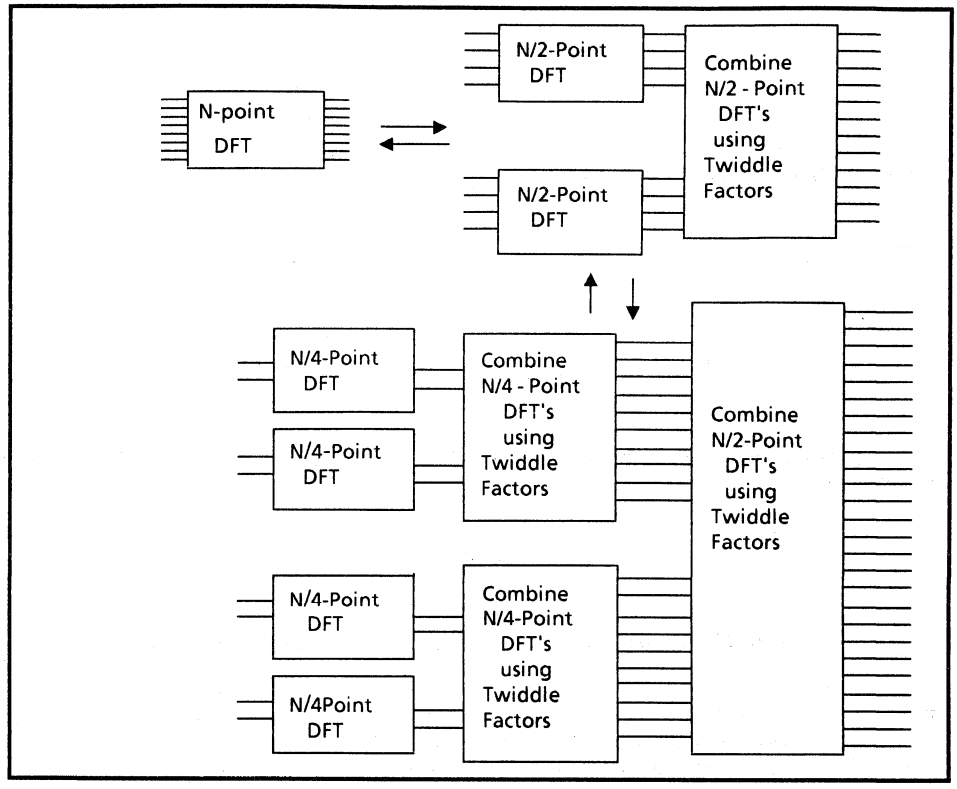


Fig 1 Typical decomposition for radix 2 FFT's

As an example, Figure 2 illustrates the splitting of an 8-point DFT into 2-point DFTs and twiddle factors.Fig 3 shows the arithmetic operations of the combined twiddle and 2-point DFT - the Butterfly

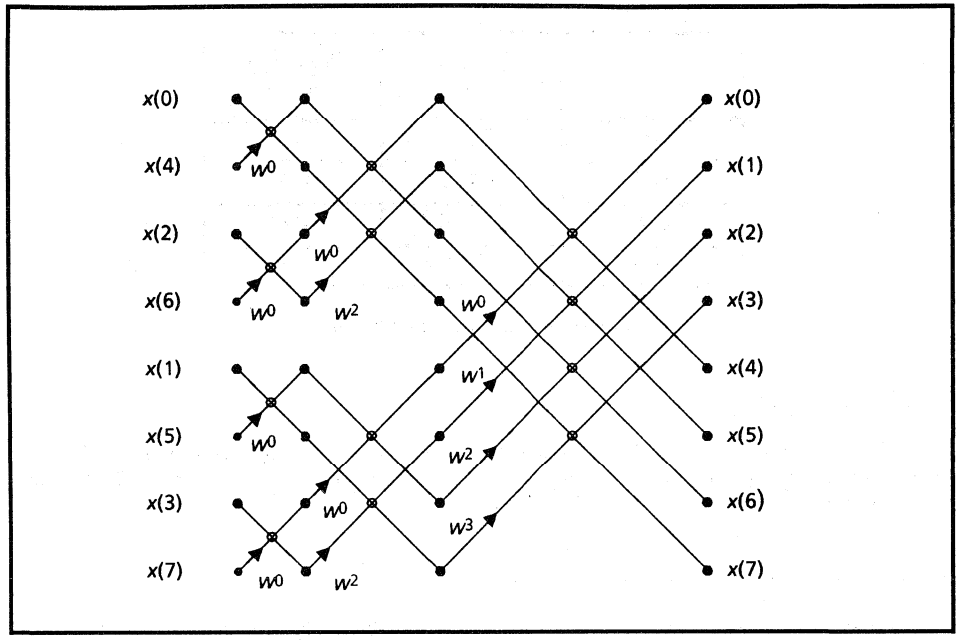


Fig 2 Eight -point FFT obtained by successive splitting into two's.

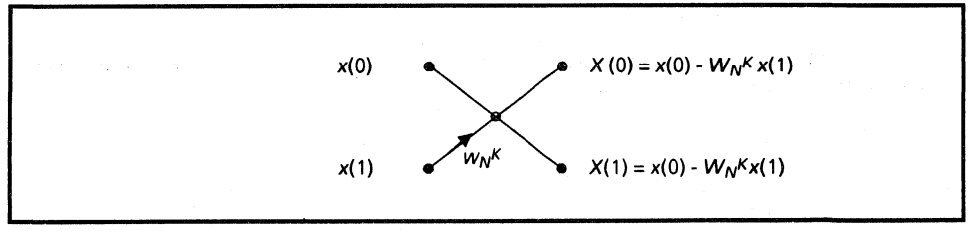


Fig 3 The Butterfly

It can be seen that as a result of this successive splitting the number of Butterfly operations is $^{N}/_{2}\log_2 N$, each Butterfly requiring only one multiplication($W_N^K x$ can be calculated and stored for use twice). Contrast this with the $(N-1)^2$ multiplications required by the direct DFT:

N	$(N-1)^2$	$^{N}/_{2}\log_2 N$ (FFT)
16	225	32
128	16129	448
256	65025	1024
1024	1046529	5120

Number of multiplications required

1.4 REALISATION

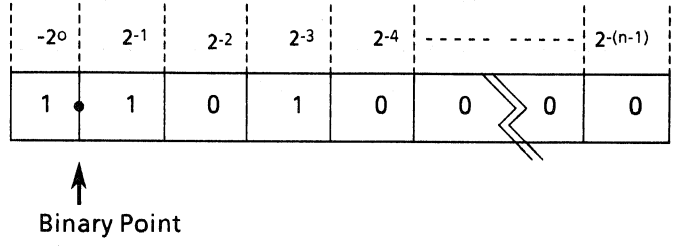
The PDSP16112 and PDSP16318 have been designed to allow the calculation of Radix 2 DIT Butterflies at very high speed. A PDSP16112A in conjunction with a pair of PDSP16318s is capable of calculating a new Butterfly every 50ns.

2.1 ARCHITECTURE AND ARITHMETIC

Figure 4 shows the basic hardware architecture of the Butterfly processor. The PDSP16112 complex multiplier calculates BW_N^K, the two PDSP16318s calculate respectively the real and imaginary parts of $A + BW_N^K$ and $A-BW_N^K$. The 12 bit input ports on the complex multiplier are used for the twiddle factors, the 16 bit ports are used for data.

2.2 ARITHMETIC CONVENTIONS

The PDSP16112 and PDSP16318 operate on 2's complement fractional data. The form of an n-bit 2's complement fractional number is:



hence 1.1010 is - 0.3750 decimal.

The number range for 2's complement fractional numbers is:

$$-1 \leq n < 1.$$

In the PDSP16112 the 28-bit multiplier results are rounded to 16 bits before entering the adders (see fig 5). The adder result is a seventeen bit number with two places ahead of the binary point, hence the output P has the range:-

$$-2 \leq P < 2$$

Fig 4 shows how the position of the binary point moves as data proceeds through the processor . The final position results from an unconditional shift at the output of the 16318s (see section 5.2), though more complex scaling strategies may be required to optimise dynamic range (see sections 5.3, 5.4, 5.5).

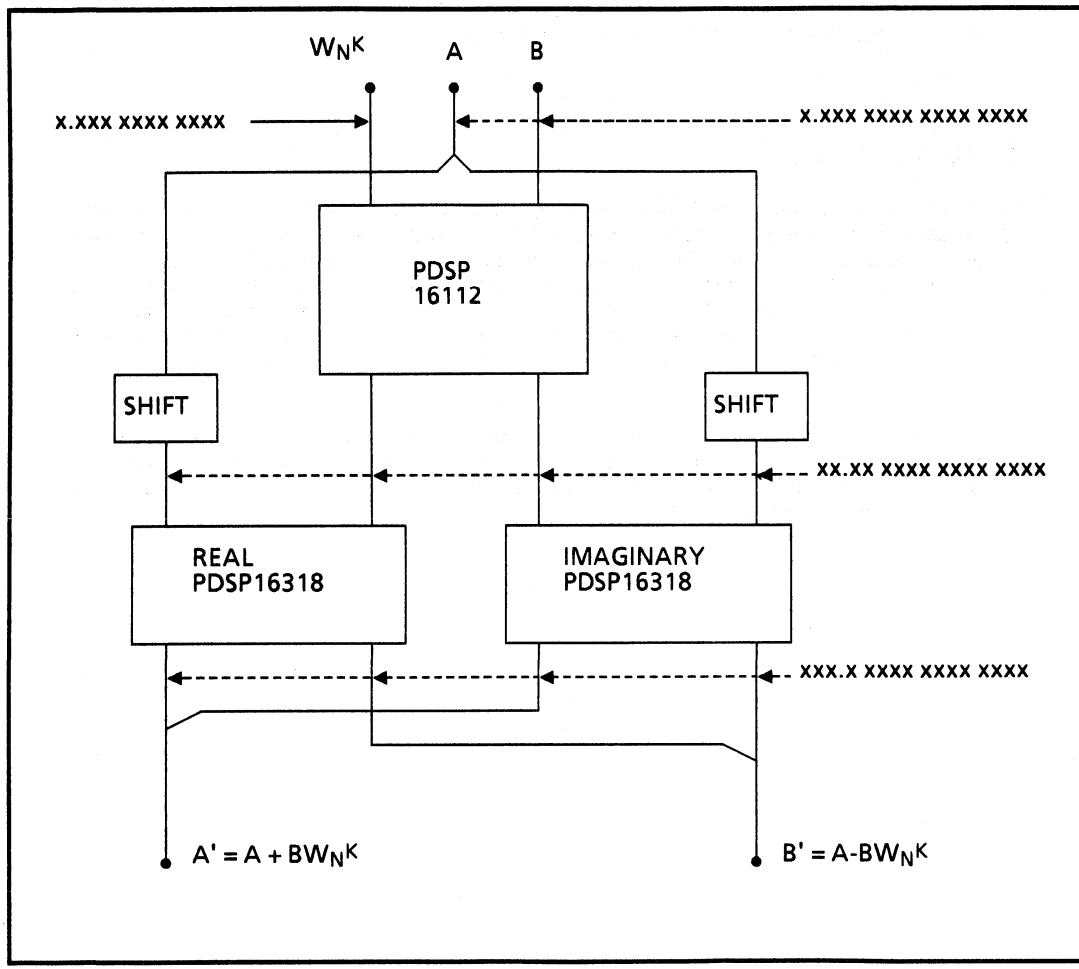


Figure 4 Basic arrangement of butterfly processor

3.1 HARDWARE

Figures 5-6 show the block diagrams of the PDSP16112 Complex Multiplier and PDSP16318 Complex Accumulator. As can be seen in Figure 5, there are a total of eight register delays in the data path through the complex multiplier. This pipeline delay would normally cause difficulties with addressing since the A and BW_N^K being presented to the 16318s would be eight cycles apart. This difficulty is avoided by the optional eight cycle delay on the 'A' port of the PDSP16318 which ensures that A and BW_N^K are presented to the adders together.

The structure of the PDSP16318 has been arranged such that a single PDSP16318 can be used with a PDSP16112 to form a complex MAC for filtering or correlation applications, or as in this case, a pair of PDSP16318s are used to handle real and imaginary data, with the internal adders performing complementary operations of A + B and A - B.

4.1 CIRCUIT DETAILS

Figure 4 shows the detailed circuit of the Butterfly Processor. The magnitude range at the output of the Complex Multiplier is ± 2 represented as a 17-bit word. The top 16 bits of this word are routed to the B inputs of the Real and Imaginary 16318s, the LSBs being left unconnected. A corresponding shift must be applied to the A inputs to the 16318s in order that data words of the same weighting are presented to the adders. This is achieved by routing the most significant 15 bits of the real and imaginary components of the "A" data into the least significant 15 bits of the A inputs on the Complex Accumulators. Input A_{15} must be connected to input A_{14} to provide sign extension for the shift.

Table 1 shows the functions of the various control lines on the 16318: DEL is active so that the 8-register delay is present in the "A" data path. ASR 1:0 are set so that the "A" adder gives A + B at its "C" output and ASI are set to give A-B at the "D" output. MS is set low to disable the accumulator feedback paths.

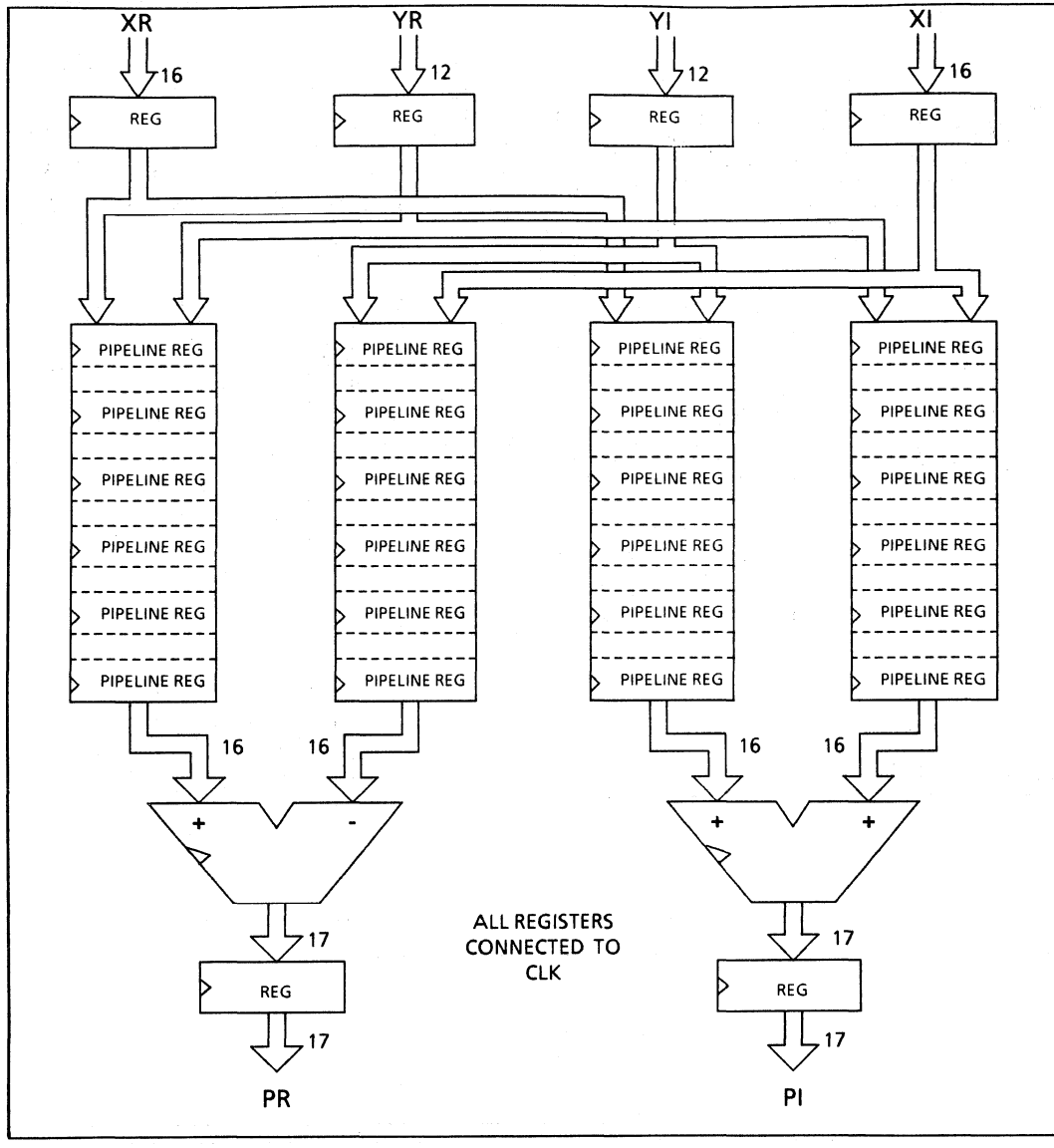


Fig.5 Pipelined multiplier structure of complex multiplier

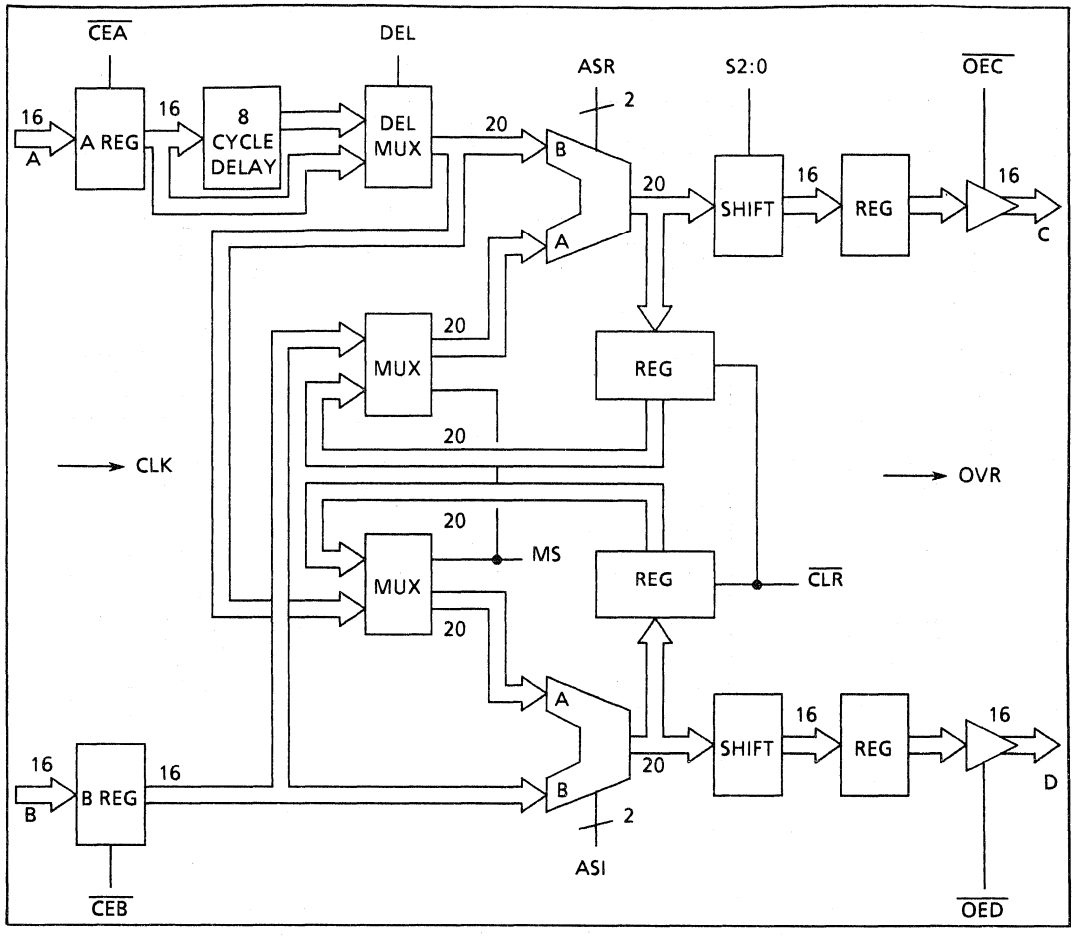


Fig.6 Block Diagram of Complex Accumulator

ASR or ASI ASX1	ASXO	ALU Function
0	0	A + B
0	1	A
1	0	A-B
1	1	B-A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MS	Real and Imag' Mux Control
0	B port input / Del mux output
1	C accumulator / D accumulator

Table 1

5.1 WORD GROWTH

Word growth in the accumulators can be accommodated by the use of the Output Shifters. Since overflows can occur independently in either the real or imaginary 16318s, the two OVR overflow flags are ORed to generate a composite overflow warning. Table 2 shows the operation of the output shifter, note than an overflow will be flagged if a shift is selected which results in the MSB of the data being outside the output range. The Shift Control lines of the Real and Imaginary Complex Accumulators must be connected in parallel, otherwise the real and imaginary data components will have different weightings, causing invalid results on subsequent operations.

The simplest scaling scenario is to select the least significant seventeen bits of the adder result (shift code 011 in Table 2). This has the effect of adding another fixed shift of one place, and will prevent any possibility of an overflow in the adder output. This unconditional shifting will produce acceptable results most of the time, though in some situations where there is significant wideband noise the signal data may be scaled down by an excessive amount. Each pass through the Butterfly Processor will cause data to be scaled down by 2 bits.

Another method of scaling is to apply no shift at all at the output of the accumulator. This option is vulnerable to an overflow occuring within the accumulator. If overflow occurs an incorrect result is output from the Complex Accumulator, however the overflow flag of the Complex Accumuator flags the invalid data which may then be corrected by external circuitry, or discarded. Further overflow risk may be minimised by scaling down the input data before passing it to the FFT processor. This will globally reduce the data magnitude and hence reduce the probability of an overflow occurring.

A third solution is a compromise between the first two. A large FFT involves several passes through the data, for example a 1K Complex FFT requires ten passes. Situations that require scaling after every pass are rare, as are situations that require no scaling at all. The compromise solution is to select different shifts of the output data from the Complex Accumulator on alternate cycles, so that on the first, third, fifth etc passes data is not shifted on the way out of the Complex Accumulator, and on the second, fourth, sixth etc data is shifted down by one place. Experimentation with real data as opposed to test signals will reveal the optimum solution for each application, the overflow flags from the Complex Accumulators warning when overflows have occurred.

There are even scenarios when the scaling introduced by the Complex Multiplier is too much and output data from the Complex Accumulators needs to be scaled up. In these situations upward scaling of the Complex Accumulator outputs can be selected, indeed an adaptive scaling system could be constructed whereby the largest output from each FFT is monitored and the scaling is adjusted up or down accordingly.

S2:0			Adder Result																		
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2 1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3 2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4 3

NOTE: This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected, the ouput data is padded with zeros

Table 2

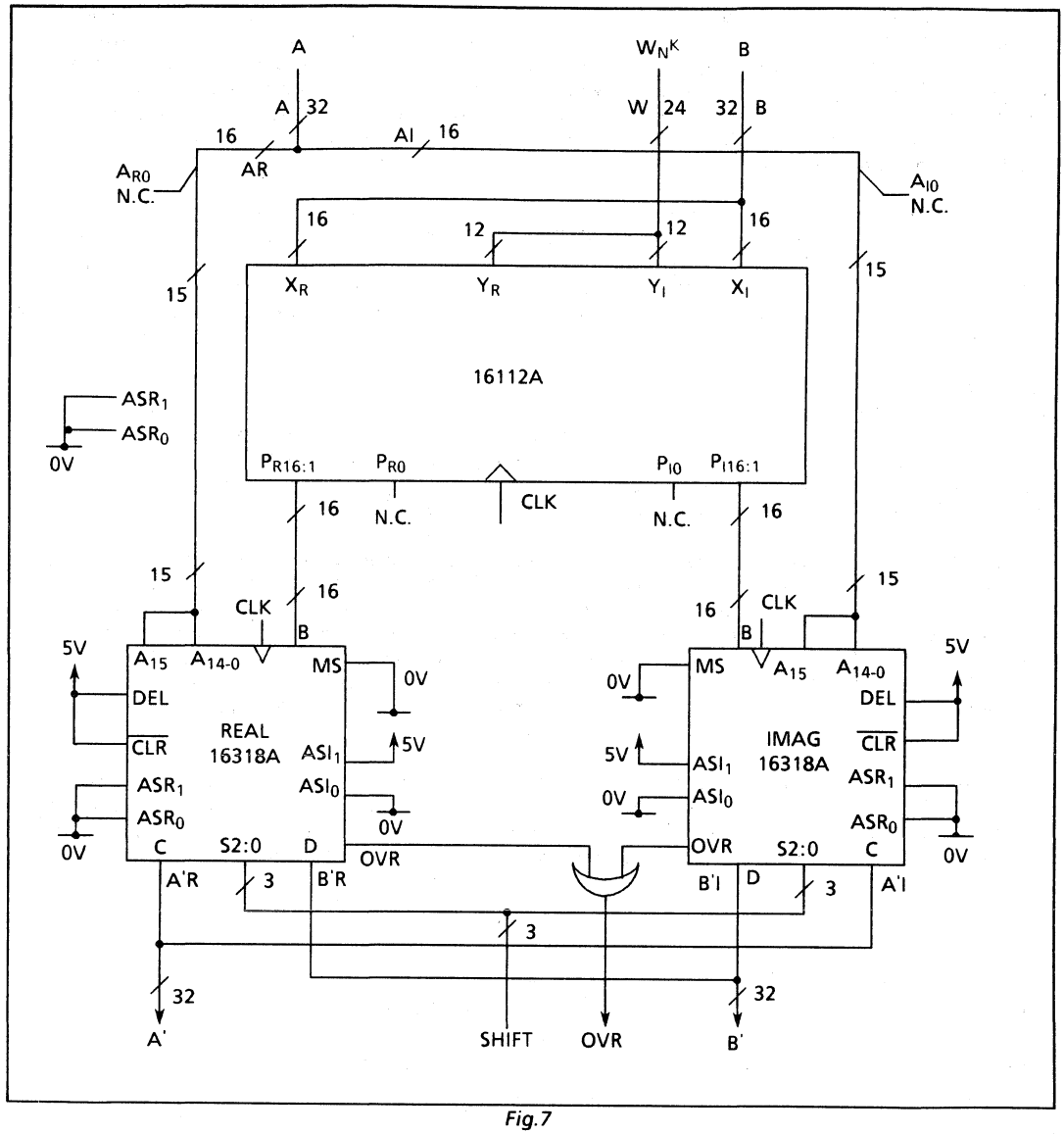

A
W_N^K
B
A 32
W 24 32 B
16
AR
AI 16
A_R0
N.C.
A_I0
N.C.
16
12
12
16
15
X_R
Y_R
Y_I
X_I
15
16112A
ASR_1
ASR_0
0V
P_R16:1
P_R0
P_I0
P_I16:1
16
N.C.
CLK
N.C.
16
15
CLK
16
16
CLK
15
B
B
5V
A_15
A_14-0
MS
0V
DEL
REAL
16318A
CLR
ASI_1
5V
ASR_1
ASI_0
ASR_0
0V
0V
C
S2:0
D
OVR
A'R
3
B'R
3
32
A'
SHIFT
OVR
B'
0V
MS
A_15
A_14-0
5V
DEL
0V
IMAG
16318A
CLR
5V
ASI_1
ASR_1
0V
ASI_0
ASR_0
OVR
S2:0
C
0V
B'I
D
3
A'I

Fig.7

6.1 PROCESSOR TIMING

The circuit of Figure 7 will operate with clock frequencies up to 20MHz if /A version parts used (10MHz for normal grade devices). The total latency is 9 cycles from inputs to outputs. The I/O timing of the processor is as follows (/A version devices, normal figures in brackets)

V_{cc} = 5v ± 10%, T_{amb} -40°C to 85°C	VALUE			
PARAMETER	MIN	MAX	UNITS	CONDITIONS
Input to CLK set up time	20(30)		ns	
CLK to Input hold time	5(8)		ns	
CLK to Output delay time		25(40)	ns	2 x LSTTL + 20pF
CLK MARK/SPACE ratio	40	60	%	

COMPLEX SIGNAL PROCESSING WITH THE PDSP16000 FAMILY

The PDSP16112 Complex Multiplier, PDSP16318 Complex Accumulator and PDSP16330 Pythagoras Processor are DSP building block parts with the unique capability of operating directly on complex data. Using conventional building blocks it is possible to operate on complex rather than real data, but at the expense of substantially reduced throughput.

Complex signal processing (where the signal comprises both in-phase and quadrature components) is necessary in signal processing applications where the phase of the signal is important. The following example illustrates such a case, and shows how the PDSP16000 devices fit into a typical DSP processor.

Consider the demodulator configuration of Figure 1.

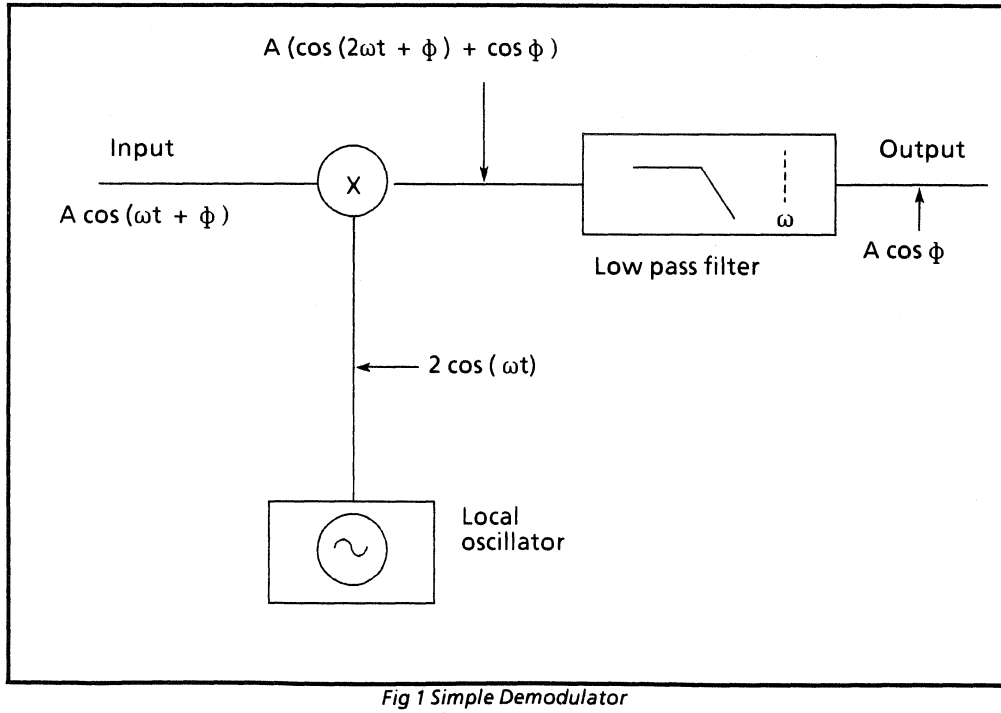


Fig 1 Simple Demodulator

The incoming signal Acos (wt + ϕ) is mixed with the output of a local oscillator running at the same frequency ω. The output from the multiplier A(cos (2 ωt + ϕ) + cos ϕ) is low pass filtered to give the baseband output Acosϕ. This is all well and good if the relative phase of the incoming signal to the L.O. is zero, but unfortunately this cannot be guaranteed. If the phase ϕ is π /2 then the demodulator output will be zero, not very useful! In a real system the relative phase between received signal carrier and local oscillator will vary, giving rise to a variety of undesirable effects from signal fading to noise on the output.

By using complex arithmetic it is possible to demodulate the received signal without phase coherence problems. Fig 2 shows an I/Q Demodulator.

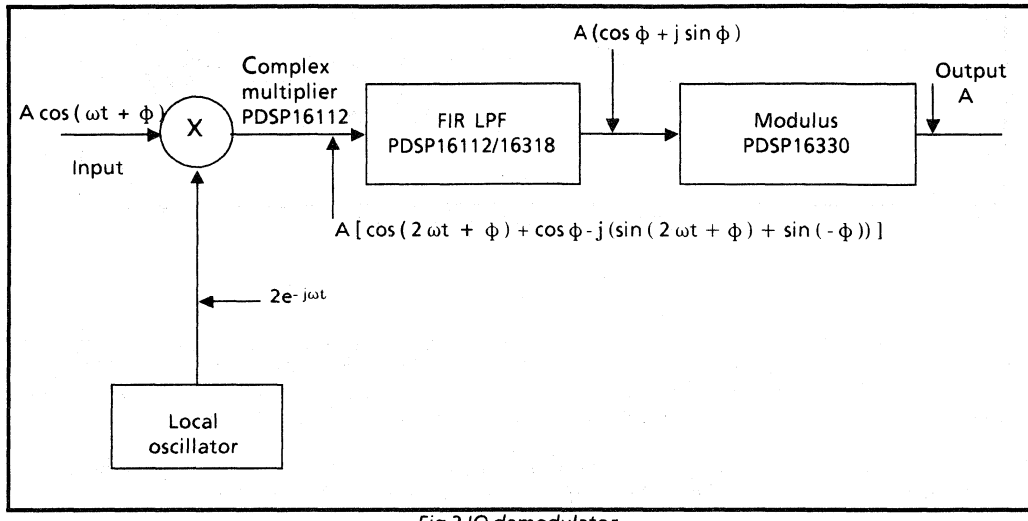


Fig 2 IQ demodulator

The output of the local oscillator is now a complex number 2 (cos ωt - j sin ωt) which is multiplied by the incoming signal in a COMPLEX MULTIPLIER such as the PDSP 16112. The complex result is then filtered to remove non-baseband signals, leaving a result A (cos ϕ + j sin ϕ) at the output of the filter. This filter must have a cut-off frequency equal to or less than half the channel spacing in the incoming signal to maintain selectivity. The filter will be an FIR filter based on a COMPLEX MAC comprising a PDSP16112 and PDSP16318.

Fig 3 shows a PDSP16112 and PDSP16318 connected as a complex MAC. For maximum accuracy the top 12 bits of the X inputs are used, and the LSB of the outputs discarded. Word growth in the accumulator is handled by the use of the output shifter on the PDSP16318

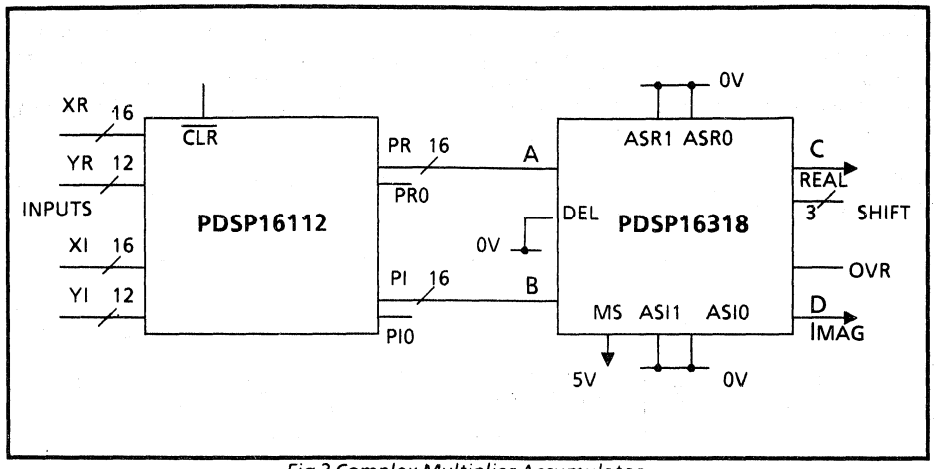


Fig 3 Complex Multiplier Accumulator

Extraction of the modulation from the complex signal $A(\cos\phi + j\sin\phi)$ is achieved by the use of PDSP16330 Pythagoras Processor. This device calculates $\sqrt{(X^2 + Y^2)}$, if $X = A\cos\phi$ and $Y = A\sin\phi$ then the MODULUS output from the PDSP16330 will be $\sqrt{(A^2\cos^2\phi + A^2\sin^2\phi)} = A$, the original modulation signal. In this case the relative phase of the carrier and local oscillator has no effect on the demodulated output.

Similar phase related difficulties are found when carring out correlation and convolution operations where complex processing is required to preserve the integrity of the signals being operated upon.

COMPLEX CORRELATION

The complex cross-correlation of two signals A and B is

$$R_{AB}(m) = \frac{1}{N}\sum_{k=0}^{N-1} \overline{A}(k).B(k+m)$$

Where A bar indicates complex conjugation, either the A or B term may be conjugated. The parameter N is the number of points over which the correlation is carried out, k and m are the sample indices.

This function can be carried out by a PDSP16112 and PDSP16318 connected as a complex MAC, k and m may be generated by PDSP1640 Address generators.

CONVOLUTION

The complex convolution of two signals A and B is defined as:

$$C_{AB}(m) = \frac{1}{N} \sum_{k=0}^{N-1} A(k) . B(m-k)$$

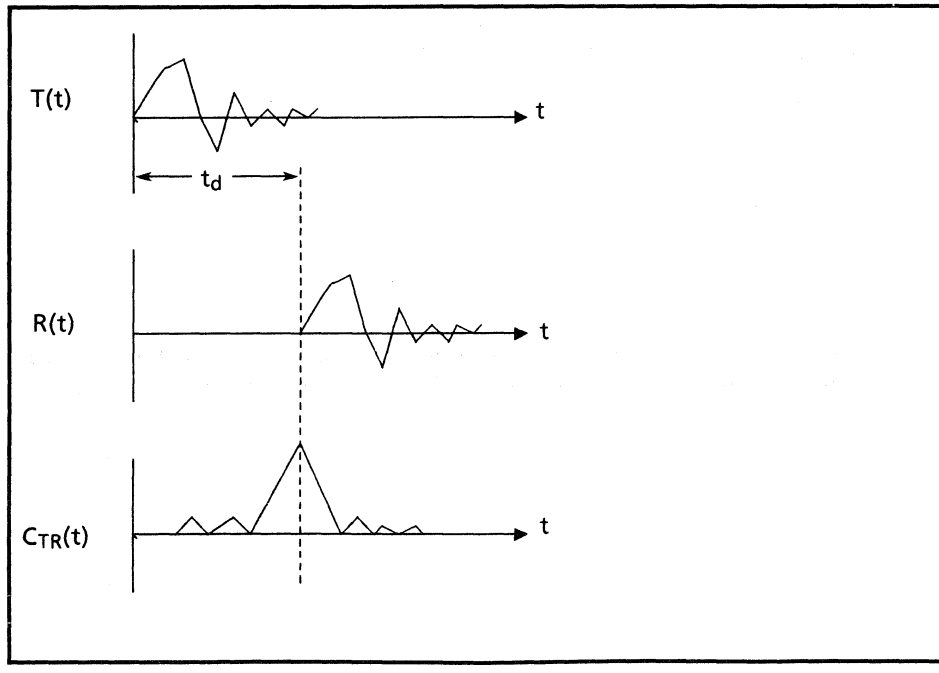
The convolution operation is, as can be seen, very similar to the correlation operation except that there is no complex conjugation involved and one of the signals (B in this case) is time reversed.

A convolver and an FIR filter are effectively the same thing. The output of a filter can be considered to be the convolution of the input and the impulse response of the filter. Because of this commonality, FIR filters, correlators and convolvers can all be performed by the same hardware systems with very little redundancy (only the complex conjugation is redundant when filtering or convolving). The time reversal required in convolution is easily achieved by programming one of the data address generators to count backwards.

APPLICATIONS OF CORRELATION / CONVOLUTION

1) DELAY MEASUREMENT

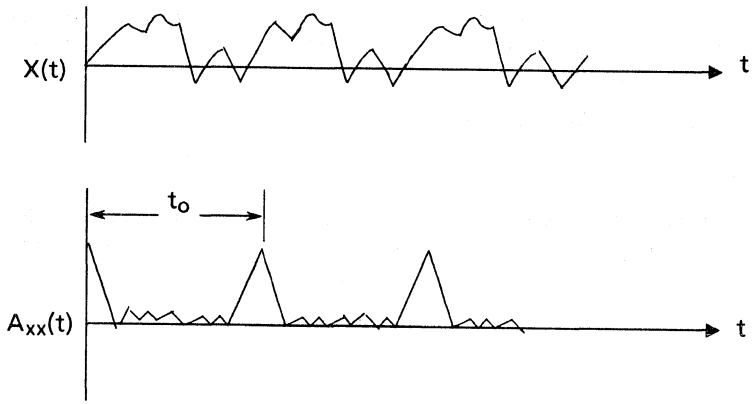
A common application of correlation in sonar, radar and geological work is the estimation of delay times. By correlating the outgoing signal with the return signal it is possible to estimate the delay between the two.



T(t) is the transmitted signel, R(t) is the returned reflection after a delay t_d. The value of t_d can be determined by the correlation of T(t) and R(t). This function will have a well defined peak at $t = t_d$ even if the signal has suffered considerable distortion on the outward and return path.

2) PITCH DETERMINATION

One of the most difficult problems in the analysis of speech or musical signals is the determination of pitch. For simple consistent waveforms, it is quite easy to determine the period - all that is necessary is to time between successive zero-crossings. With complicated waveforms this approach is no longer reliable, but autocorrection offers a workable technique.



Estimating the period of the waveform X(t) by zero-crossing timing clearly will not work as there are a number of zero-crossings per cycle. The autocorrelation function of X(t), $A_{xx}(t)$ exhibits very pronounced peaks every cycle.

3) NOISE CANCELLATION

A common difficulty in many signal processing systems is recognizing the desired signal in the presence of large amounts of masking noise. Correlation can be used to extract required signals from background noise if the appropriate characteristics of the signal are known.

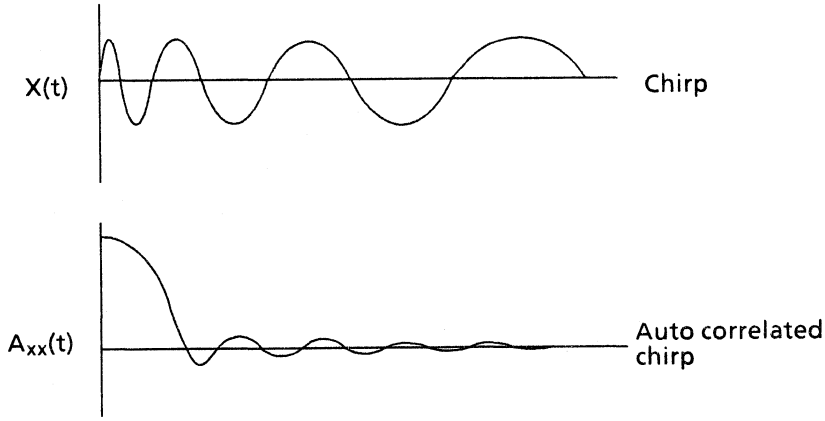
If a signal in the presence of background noise is correlated with an estimate of the signal, the required signal will correlate strongly with the estimate and weakly with the noise. The improvement on signal - to - noise ratio known as Correlation Gain, obtained by an N-point correlation is:

$$G = 10\log_{10} N \text{ dB}$$

4) PULSE COMPRESSION

In radar systems there is a design conflict between range resolution and operational range. In order to maximise operational range the average radiated power must be as high as possible. However most transmitters have limited peak power delivery which means that for maximum range, the transmitted pulse length must be as large as possible. The range resolution of the radar is $\frac{1}{2}tc$, where t is the pulse duration and c the velocity of light. For a pulse duration of 10μs, the range resolution will be 1500m, that is, two targets within 1500m of each other could not be distinguished!

Pulse compression radar operates by transmitting not a simple 'burst' but a special waveform known as a 'chirp'.



The important characteristic of a chirp is that its autocorrelation function is substantially shorter in duration than the chirp itself, the greater the swept bandwidth of the chirp, the shorter the autocorrelation pulse.

In a radar system, the transmitter sends out a linearly frequency modulated pulse of such a duration needed to obtain the required operating range. In the receiver the signal is correlated with a replica of the transmitted chirp to produce a short duration pulse, which can give good range resolution.

5) DFT

The equation for a DFT is:

$$X(k) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) e^{-j2\pi nk/N} k = 0,1,.....(N-1)$$

Contrast this with the function for convolution above:

$$C(m) = \frac{1}{N} \sum_{k=0}^{N-1} A(k).B(m-k)$$

It can be seen that the two operations are identical if B is made equal to $e^{-j2\pi nk/N}$.

Usually a DFT will be evaluated by the familiar Cooley-Tukey radix 2 FFT algorithm, but there are applications where the straightforward DFT is preferable. If the transform length is relatively short, a direct DFT using the PDSP16112 and PDSP16318 can be both cost effective (the hardware is much simpler than for FFT) and (because of the high speed of the devices) still capable of acceptable transform speeds. Unlike the Cooley-Tukey Algorithm a DFT may be of any number of points and being non-recursive, can achieve greater accuracy.

A FAST FFT PROCESSOR USING THE PDSP 16000 FAMILY

THE PROBLEM

The current industry standard benchmark for the execution of a 1024 point complex FFT is of the order of 2ms. This article describes how an FFT processor almost an order of magnitude faster may be built using Plessey's PDSP16000 family of highly integrated CMOS DSP building blocks.

Fig. 1 shows diagrammatically the fundamental operation of the FFT algorithm, the Butterfly.

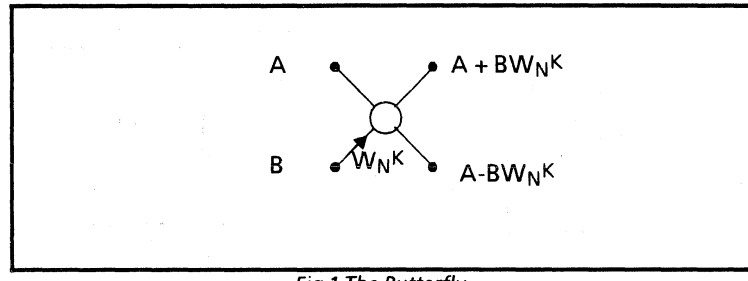


Fig 1 The Butterfly

This operation requires a complex multiply, an addition and a subtraction to complete. If we set a target of 256μs for a 1024 point FFT (roughly ten times faster than can be achieved with an FFT processor designed around a 100ns MAC), then the time allowed to calculate the Butterfly is:

$$256/(^N/_2 \log_2 N)\ \mu s \quad \text{(where N = 1024)}$$

$$= 50ns.$$

The complex multiplication operation itself requires four real multiplications, an addition and a subtraction, so that the complex Butterfly requires four multiplies, three adds and three subtractions to be executed in 50ns.

Using ECL logic and the fastest available ECL array multiplier (BIT's ECL MAC will operate at 100MHz) it is possible to construct a 50ns Butterfly Processor. The problems with this, though, are quite severe. The ECL Butterfly Processor consumes a great deal of power, require its I/O bus to operate at 100MHz and occupies a large amount of board space. Such a processor is far from simple to design and places horrendous access time requirements on external memory.

THE SOLUTION

Plessey's PDSP16000 family solution takes a very different approach to that above; at the heart of the Butterfly Processor is the PDSP16112 Complex Multiplier (Fig 2)

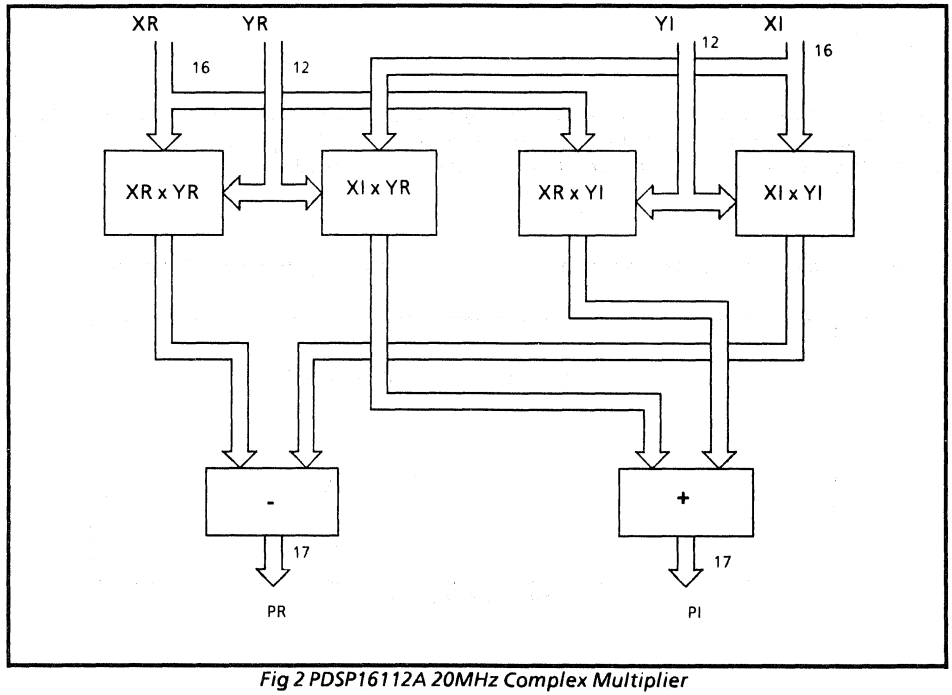


Fig 2 PDSP16112A 20MHz Complex Multiplier

This device contains four pipelined 16x12 Array multipliers, a 17-bit Adder and a 17-bit subtractor. The multipliers accept data from the X_R, X_I, Y_R, Y_I inputs and perform the four multiplies necessary to implement a complex multiplication:

$$X_R.Y_R;\ X_R.Y_I;\ X_I.Y_R;\ X_I.Y_I.$$

The 28-bit results from these operations are rounded to 16 bits before being passed to the adder and subtractor. The subtractor calculates:

$$(X_R.Y_R - X_I.Y_I) = P_R$$

to form a 17-bit real result P_R.

The adder calculates:

$$(X_R.Y_I + X_I.Y_R) = P_I$$

to give a 17-bit imaginary result P_I.

The add and subtract operations may, depending on the data, cause the results to grow by one bit (hence the 17-bit wide outputs). The PDSP16112 operates using 2's complement arithmetic, hence if fractional 2's complement is used, the outputs will lie in the range:

$$-2 \leq P < 2$$

for inputs in the range:

$$-1 \leq X \text{ or } Y < 1.$$

For outputs in the range:

$$-1 \leq P < 1$$

the 17th bit (msb) will duplicate the 16th bit (the sign bit).

Both inputs and outputs are registered. On the rising edge of the clock, data is clocked into the input registers. At the same time a new result is clocked into the output registers. The maximum clock frequency is 20MHz, giving a full complex multiply in 50ns. The final operations required in calculating the Butterfly are the addition and subtraction. The PDSP16318 Complex Accumulator (Fig 3) can be configured for these operations.

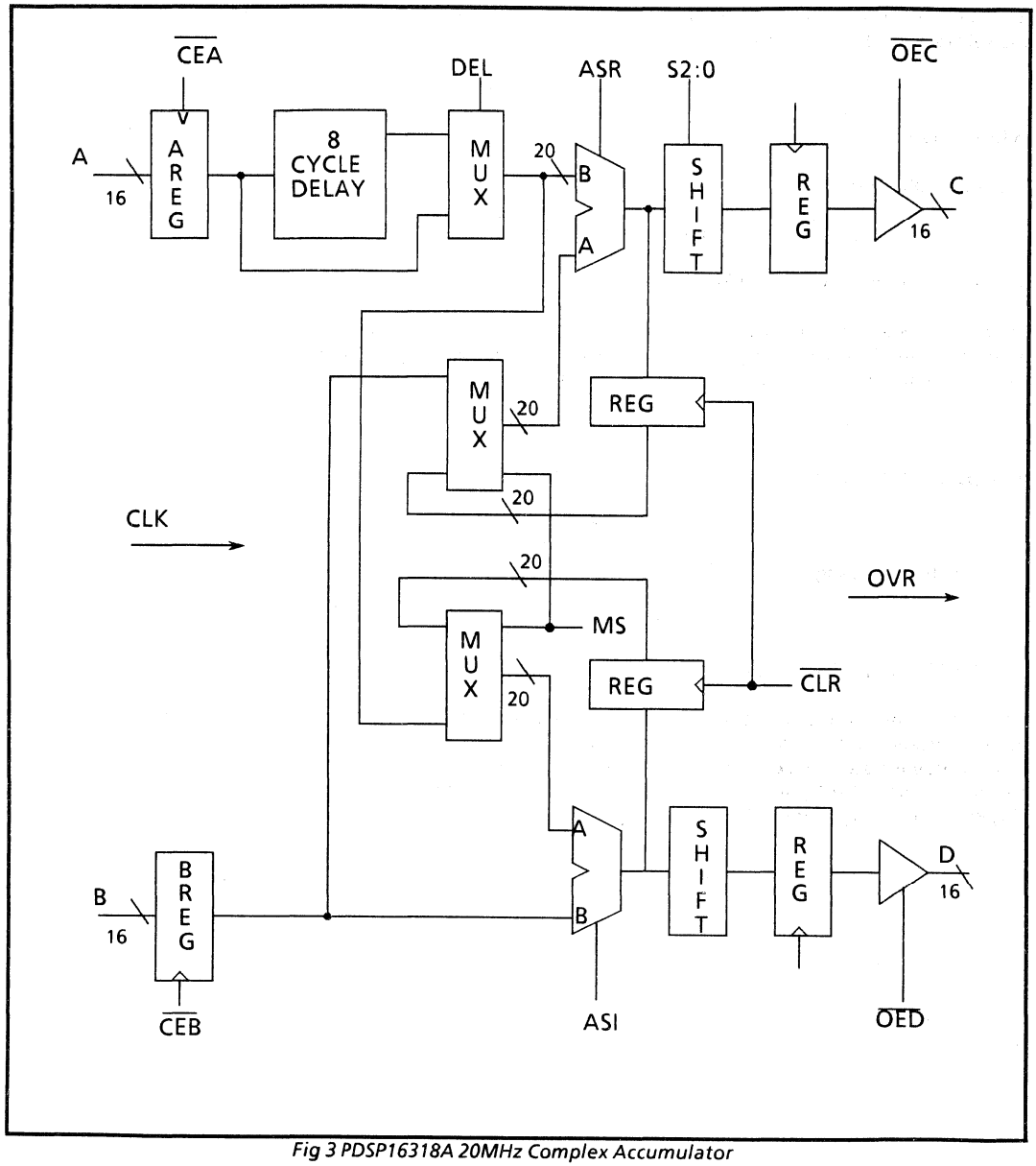


Fig 3 PDSP16318A 20MHz Complex Accumulator

This device has a variety of applications in filtering, correlation and FFT. In filtering and correlation applications, a single PDSP16318A is used in conjunction with a PDSP16112A to form a complex MAC. When used in FFT applications, a pair of PDSP16318As are used with a PDSP16112A to form a Butterfly Processor capable of executing a Radix 2 DFT Butterfly every 50ns, using 16 bit data and 12 bit twiddle factors.

Fig 4 illustrates the connections between the devices.

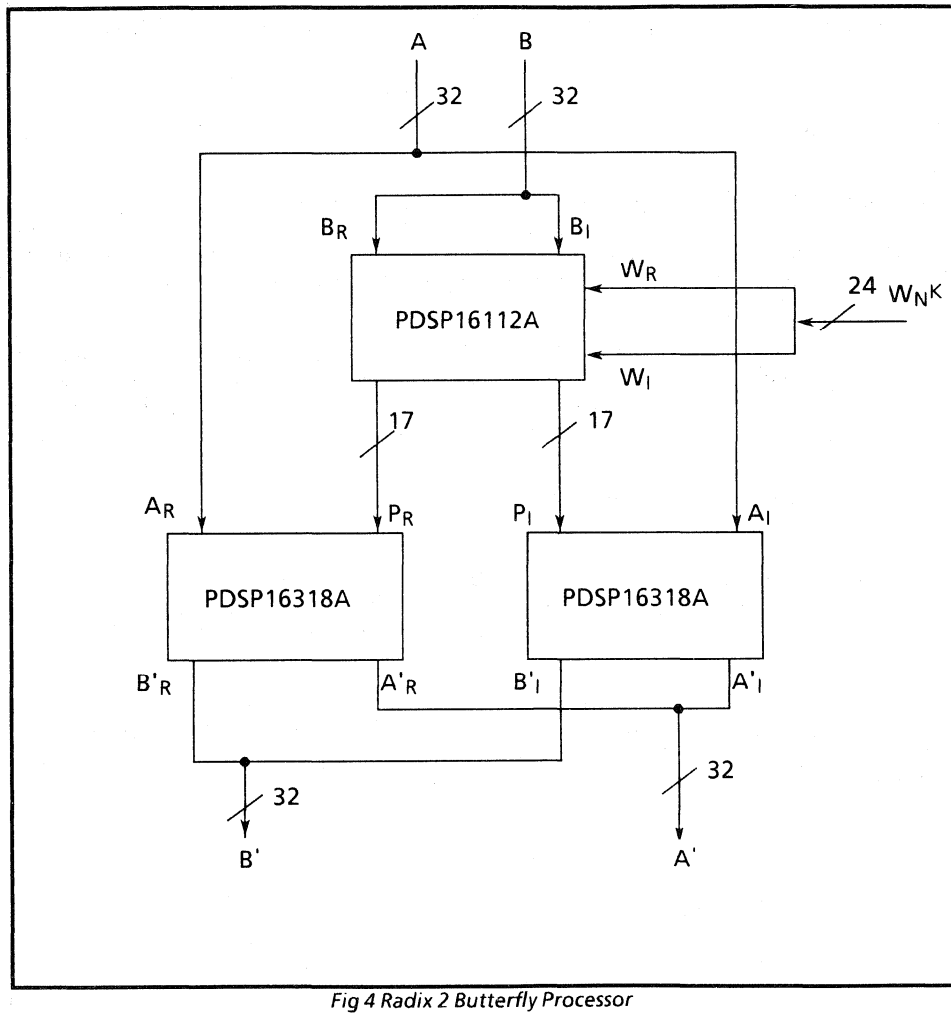


Fig 4 Radix 2 Butterfly Processor using PDSP16112A & PDSP16318A

The PDSP16112A provides the real and imaginary parts of BW_N^K to the two PDSP16318As. One of the PDSP16318As calculates the real parts of $A + BW_N^K$ and $A-BW_N^K$, the other, the imaginary parts of $A + BW_N^K$ and $A-BW_N^K$.

For even greater throughput, one chip-set (16112 + 2 x 16318) may be allocated to each column of the FFT. As an example, 10 chip-sets will allow the execution of a 1024 point complex FFT in a mere 26μs!

Application Note AN 47 'A RADIX 2 BUTTERFLY PROCESSOR' describes the Butterfly hardware in greater detail.

MEMORY REQUIREMENTS

In the 1960s, when the FFT algorithms were first being developed, memory was an expensive commodity. This led to the invention of 'In-Place' FFT algorithms in which the results A', B' of a Butterfly are put back into the locations from where the inputs A, B are read. With a Butterfly Processor as fast as the one described above, In-Place Algorithms pose a nasty problem.

Examination of Figure 4 shows that in every 50ns cycle, two reads from and two writes into memory have to be accomplished. The obvious implication is that the RAM has to have an access time less than 12.5ns. Such RAM is expensive as these speeds are right at the limits of that achievable for CMOS RAM - clearly an alternative arrangement must be found.

THE CONSTANT GEOMETRY ALGORITHM

The Constant Geometry Algorithm is illustrated in Fig 5. On each pass of the FFT, the read/write address sequence is the same, but the addresses written to after each Butterfly are different to those from where the input data is read. This requires twice as much RAM as for In-Place algorithms.

The key to the use of the Constant Geometry algorithm is the recognition of the order in which data points are addressed. Fig 5 illustrates the Butterfly structure of the Constant Geometry algorithm. For an N point transform, the read addressing sequence is:

A		B
0	and	N/2 + 0
1	and	N/2 + 1
2	and	N/2 + 2
3	and	N/2 + 3

or in general for n = 0 to (N/2-1)

the addresses are n and N/2 + n.

For the same N point transform the write address sequence is:

A'		B'
0	and	1
2	and	3
4	and	5
6	and	7

or in general for n = 0 to (N/2 - 1),

the write addresses are 2n and 2n + 1.

MEMORY CONFIGURATION

The implication so far is that four memory accesses are required every cycle, which is only 50ns long hence needing 12.5ns memory cycles! The reality is that four separate blocks of RAM may be configured as one in such a way that any given device is only accessed twice for each four access Butterfly cycle.

This reduces the required access time to only 25ns which is feasible with current RAM devices. The required RAM bandwidth may be reduced by a further factor of two to a more comfortable 50ns by 'double buffering', ie using two banks of storage, one for reading and one for writing. After each pass these storage banks swap roles, data being passed back and forward between them via the Butterfly Processor. This step doubles the amount of RAM required, but reduces each RAM device's required I/O bandwidth by a factor of two, to one cycle every 50ns.

Half of the required memory configuration is as shown in Fig 6. This structure is duplicated, each half alternating between sourcing and receiving data to and from the Butterfly Processor.

Each memory is divided up into four quadrants each quadrant being a separate 32-bit block of RAM with separate input and output ports. The two left hand quadrants are configured to accomodate data points with even valued addresses, the right quadrants accomodating data points with odd valued addresses. The upper two quadrants accomodate data points with address values greater than (N/2-1), where N is the transform size, the lower two quadrants accomodate data points with addresses with values less than or equal to (N/2-1).

The left hand quadrants have their inputs commoned to become the "A'" input bus, the right hand quadrants have their inputs commoned to become the "B'" input bus. The upper quadrants have their outputs commoned to become the "B" output bus, and the lower quadrants have their outputs commoned to become the "A" output bus. These buses are connected to the Butterfly Processor "A',B',B,A" output and input buses respectively.

The mode of addressing the composite RAM is suprisingly simple as each quadrant is supplied with exactly the same address.

The example of Fig 7 shows the storage of data points for a 16 point transform according to the Even-Odd (N/2-1) rules. These 16 data points are addressed two at a time by the 8 term address sequence 0,0,1,1,2,2,3,3 or the address sequence 0,1,2,3,0,1,2,3 depending upon whether reading or writing is required. Unlike all other FFT algorithms, this address sequence remains unchanged thoughout each pass of the transform.

Reading Mode.

When reading data from the RAM, quadrants enabled alternate between the left and the right pairs of quadrants and the address sequence used is 0,0,1,1,2,2,3,3. As can be seen from the example in Fig 7 this simple count sequence on the address port will result in the data points read onto the A and B buses being:

A		B
0	and	8 on the 1st cycle with the left quadrants enabled
1	and	9 on the 2nd cycle with the right quadrants enabled
2	and	10 on the 3rd cycle with the left quadrants enabled
3	and	11 on the 4th cycle with the right quadrant enabled
4	and	12 on the 5th cycle with the left quadrant enabled
5	and	13 on the 6th cycle with the right quadrant enabled
6	and	14 on the 7th cycle with the left quadrant enabled
7	and	15 on the 8th cycle with the right quadrant enabled

Write Mode.

When writing data to the RAM the quadrants enabled are the lower pair for the first half of the operation and the upper pair for the second half of the operation. The address sequence used is 0,1,2,3,0,1,2,3. As can be seen from the example in Fig 7, this simple count sequence on the address port will result in the data points written into the RAM from the A' and B' buses in the following manner:

A'		B'
0	and	1 on the 1st cycle with the lower blocks enabled
2	and	3 on the 2nd cycle with the lower blocks enabled
4	and	5 on the 3rd cycle with the lower blocks enabled
6	and	7 on the 4th cycle with the lower blocks enabled
8	and	9 on the 5th cycle with the upper blocks enabled
10	and	11 onthe 6th cycle with the upper block enabled
12	and	13 on the 7th cycle with the upper blocks enabled
14	and	15 on the 8th cycle with the upper blocks enabled

Reference to the Constant Geometry diagram of Fig5 will show that this address sequence is as required by the algorithm. Each separate RAM package is only accessed once each cycle resulting in 50ns access time RAM being sufficiently fast for this speed application.

ADDRESSING

The addressing sequence of the data RAMs can be totally satisfied by a PDSP1640A 40 MHz Address Generator. The PDSP1640 (see Fig 8) integrates an eight bit add-latch loop with an on chip comparator and five user programmable registers. The PDSP1640A occupies a 28 pin package which in LCC form offers the smallest footprint of any Address Generator.

COEFFICIENT ADDRESSING

The coefficient addressing sequence required by the Constant Geometry Algorithm is as simple as the Data Addressing sequence. The correct sequence for a normally ordered input, bit reversed output Forward Transform is as illustrated in Fig5.

To generate the sequence of values of K for the coefficients W_N^K in Fig 5 use the following routine:

$$K = \text{Bit Reversed } [0,....(2^{(m-1)}-1)]$$

this sequence is repeated $\frac{1}{2}$ N.2^{m-1} times where m is the column number of the FFT and N is the number of points.

Thus for 16 points, for example, the sequence on the 4th pass is given by the count sequence of 0 to (2 to the power 3) - 1 = 7 is repeated (16/2) / (2 to the power 3) = once.

This count from 0 to 7 is then bit reversed to give 0,4,2,6,1,5,3,7 as shown in Fig 5.

The coefficients need to be accessed on the same 50ns cycle as data, requiring the use of RAM as the storage medium. The Address sequence is easly generated by a pair of PDSP1640A's which will address a 16 bit field at speeds in excess of 20MHz. The output of the PDSP1640A's is wired in bit reversed order before being applied to the Coefficient RAMs.

FFT PROCESSOR CONFIGURATION

The architecture of the complete FFT processor is as shown in Fig 9. Each of the two data RAMs is addressed by its own PDSP1640A address generator, as is the coefficient RAM. A configuration using 50ns access 256 word RAM devices, each addressed by a single 8 bit wide PDSP1640A, will in conjunction with PDSP16112A and PDSP16318A Arithmetic processors execute a 1024 point Complex FFT in just 256μs, a solution that is realised entirely with CMOS Logic, fits on a single board yet deliveres a benchmark eight times faster than the Industry Standard.

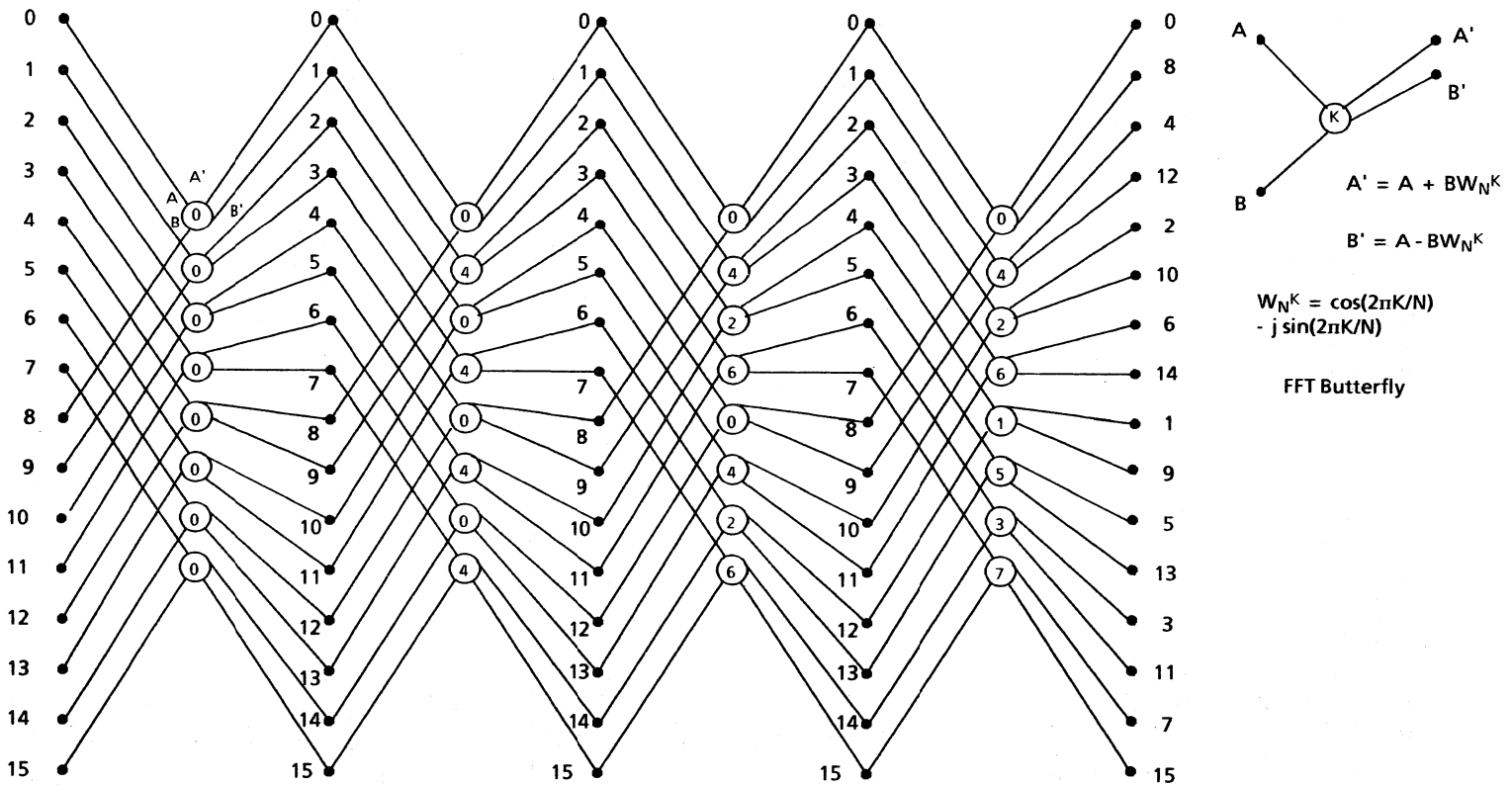


Fig 5 16 point constant geometry DIT Radix 2 algorithm

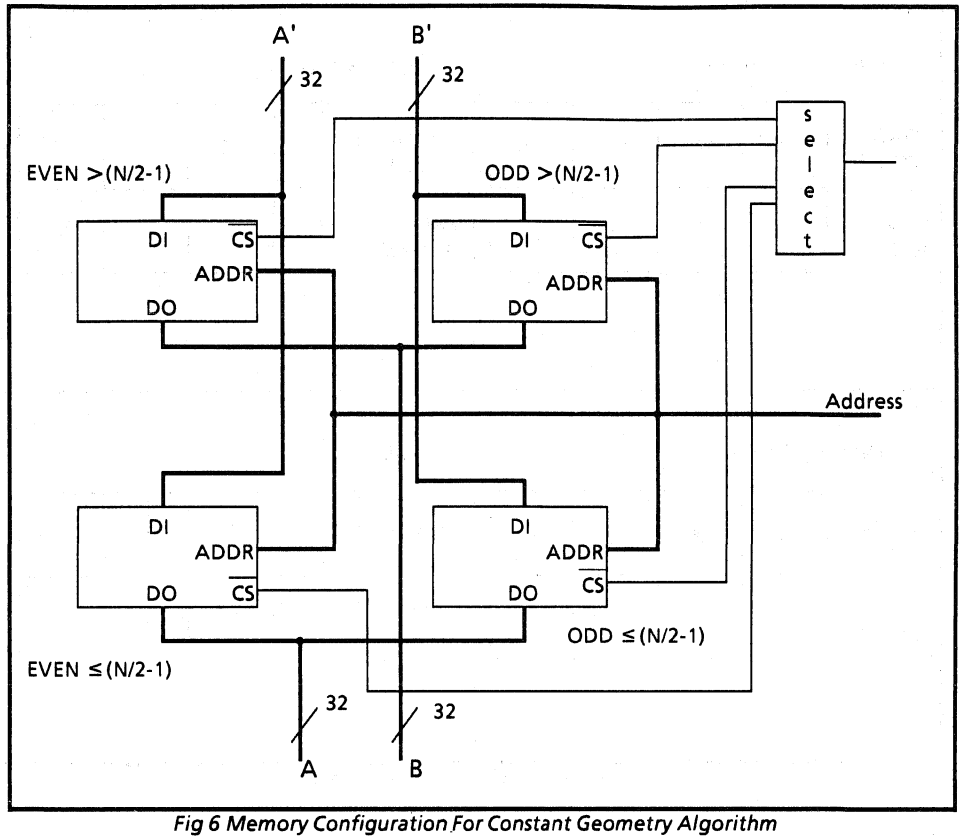


Fig 6 Memory Configuration For Constant Geometry Algorithm

The memory is configured in four quadrants each comprising 32 bit wide blocks of RAM. All four quadrants share the same Address Bus and Read/Write select lines. Each quadrant is independently enabled via its chip select control.

The blocks of RAM have seperate Read and Write Data ports which are connected to the A,B,A',B' Butterfly Processor ports as indicated.

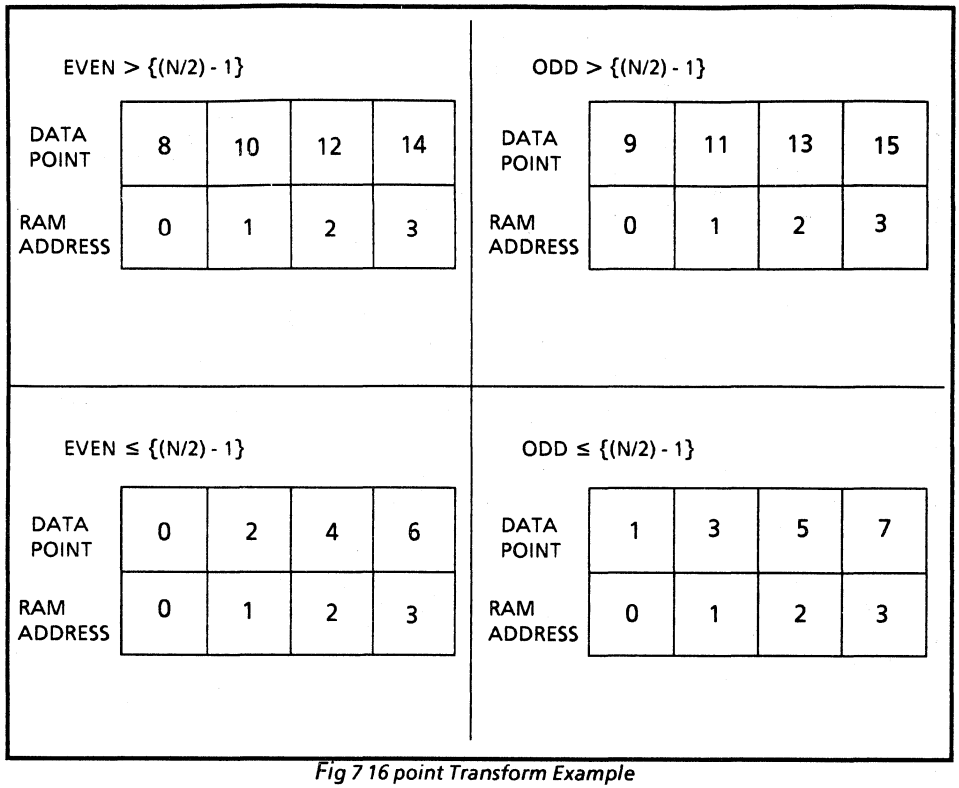


Fig 7 16 point Transform Example

The data points of a 16 point transform are stored in the four RAM quadrants at the addresses and in the quadrants indicated.

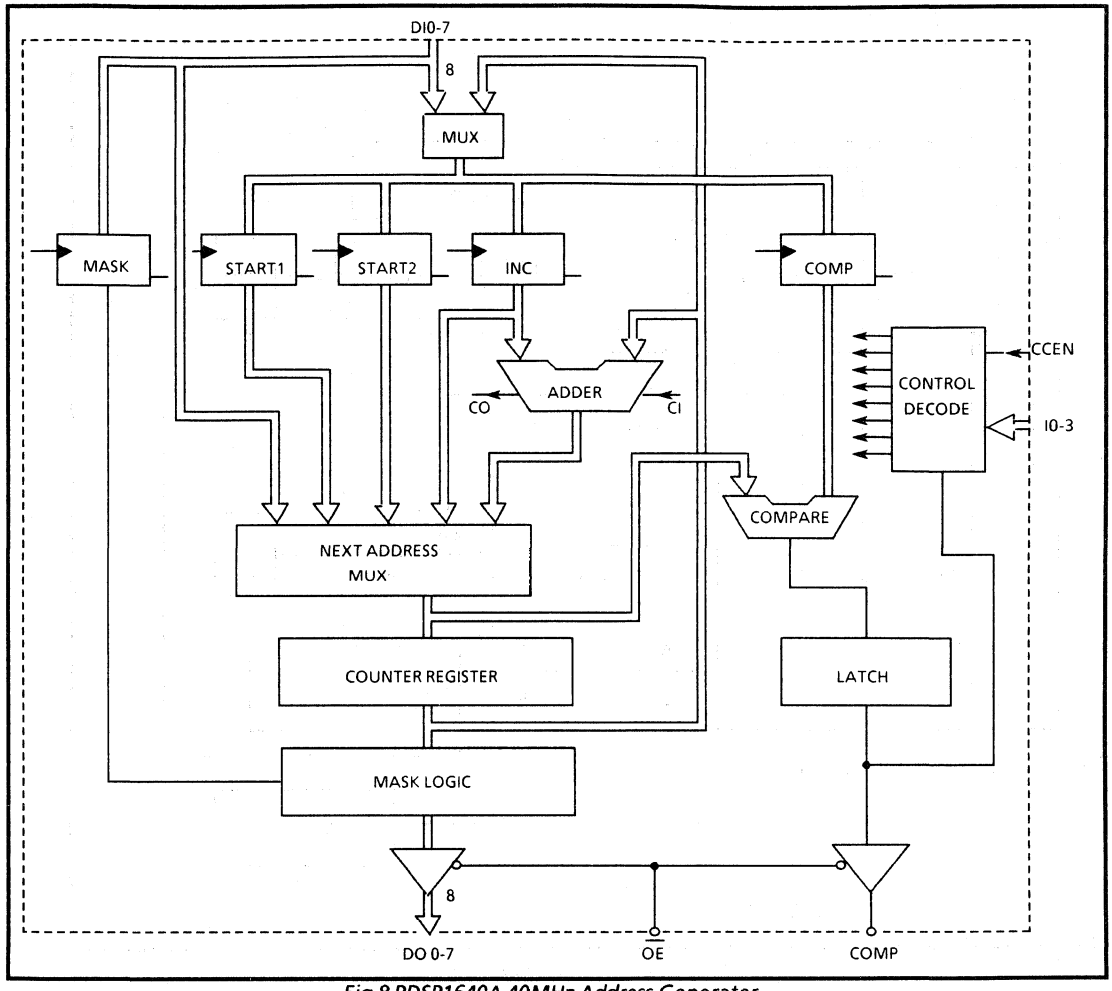


Fig 8 PDSP1640A 40MHz Address Generater

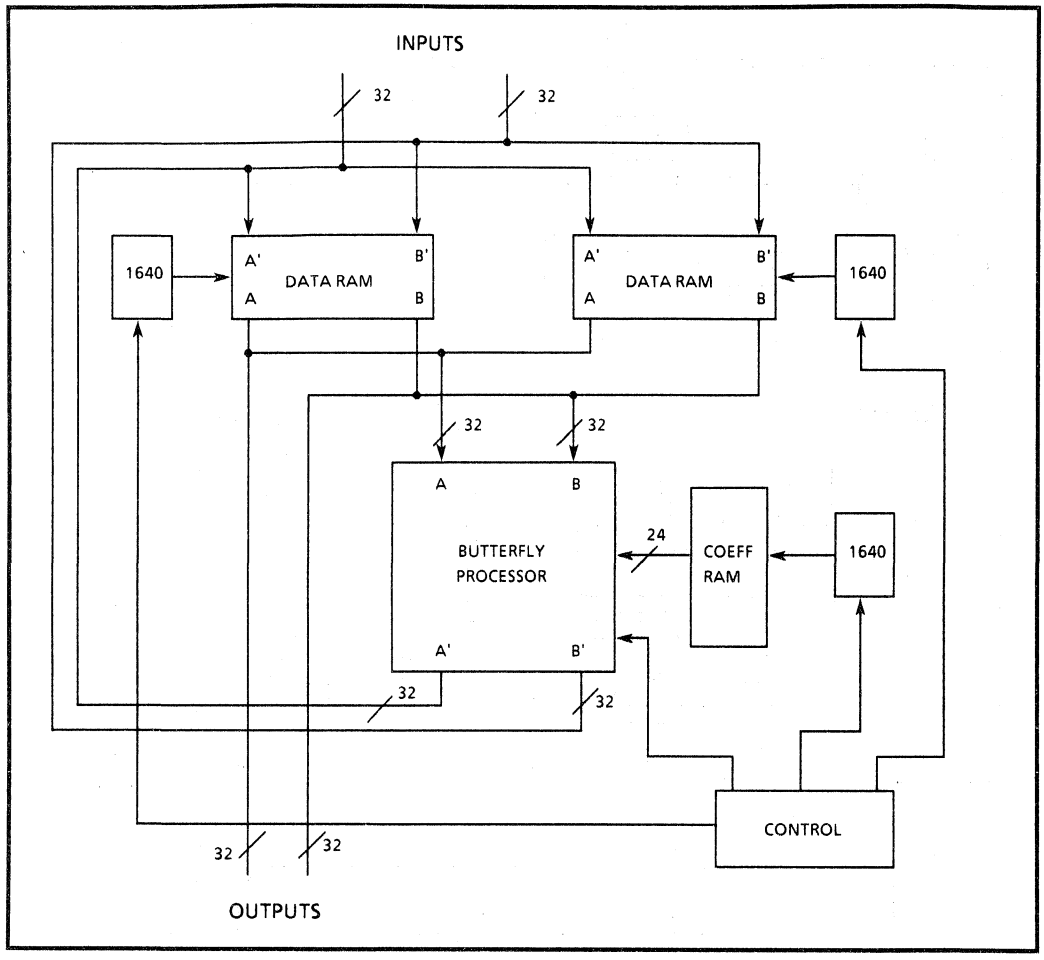


Fig 9 FFT Processor Architecture

FFT ADDRESS GENERATION USING PDSP1640

1.1 Introduction

Fast Fourier Transforms (FFTs) are used in a wide variety of applications as a means of calculating the Discrete Fourier Transform of a signal, in order to estimate the signal's spectral energy. There are many different algorithms for computing FFTs, each designed to exhibit particular characteristics, but each of which also have certain disadvantages. The in-place radix 2 DIT algorithm shown in fig 1, puts the outputs from each stage into the same memory location from which the inputs are read. This minimises the system memory requirements, but has the disadvantage of requiring a different register addressing sequence at each stage and also requires four memory accesses per butterfly cycle, necessitating the use of very fast RAM.

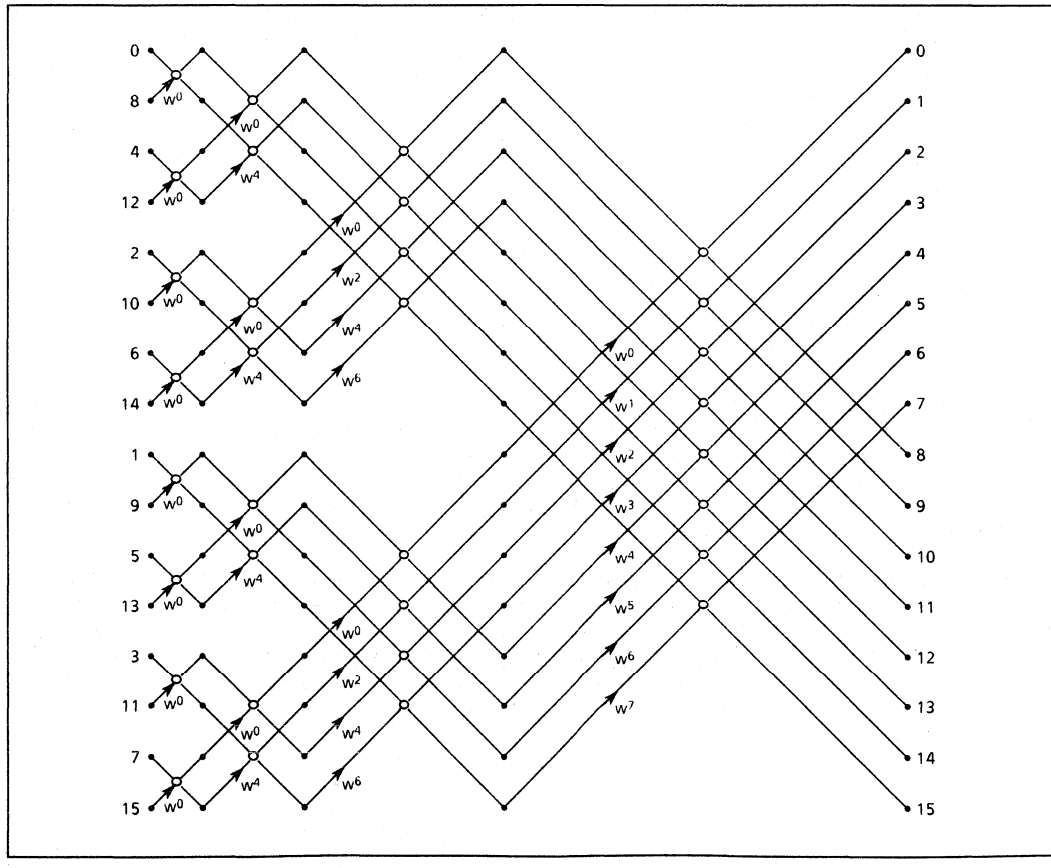


Fig 1. 16-Point In-Place Radix 2 DIT FFT Algorithm

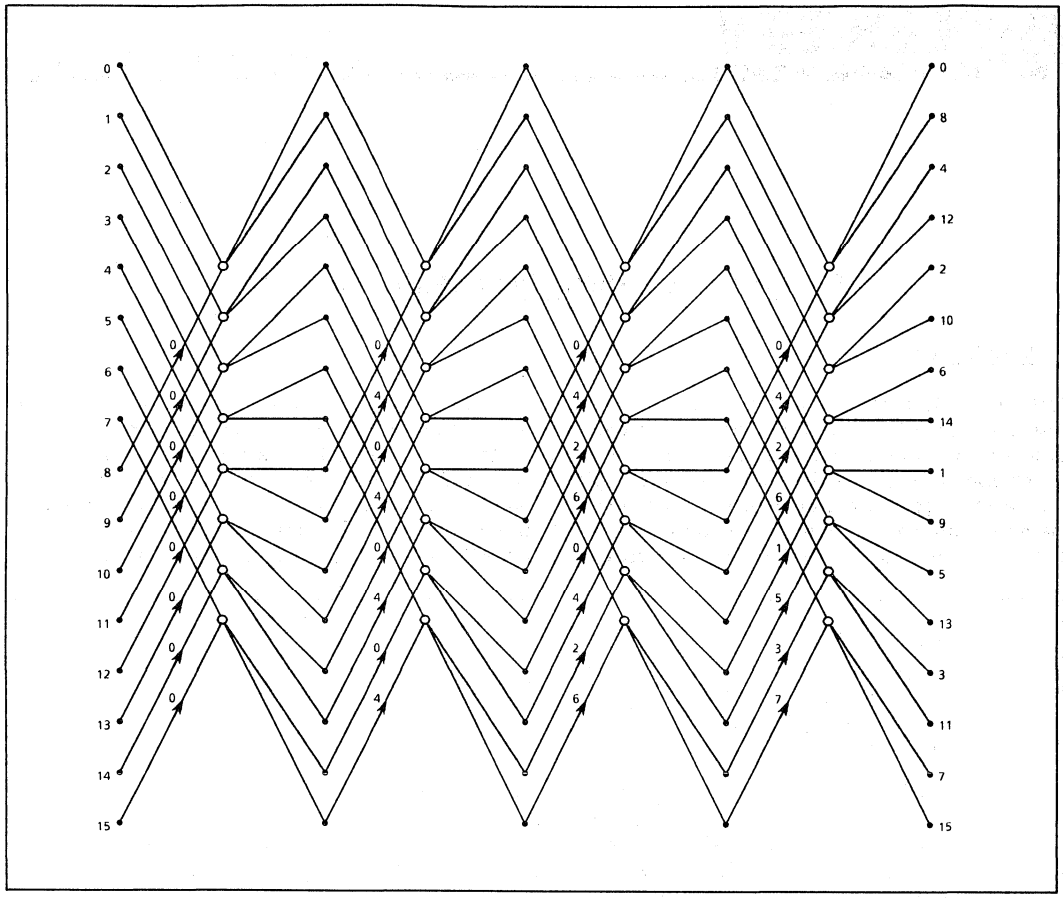


Fig 2. 16 Point Constant Geometry Radix 2 DIT FFT Algorithm

The main advantage of the 'constant geometry' algorithm, shown in fig 2, is that the data memory may be configured such that any particular RAM device need only be accessed once during each butterfly cycle, thus allowing the use of slower devices. The algorithm also has the feature that the memory read address sequence and the memory write address sequence remains the same from one stage to the next. However, the algorithm is not in-place and therefore requires twice as much RAM storage as an in-place algorithm and the coefficients are not in a simple order.

These two algorithms are, perhaps, the most common of FFT algorithms and as such are used in this Application Note as examples of the FFT Address Generation capabilities of the PDSP1640. The variety of FFT algorithms available shows that the data and coefficient address sequencing is a major consideration in the implementation of any one, requiring in nearly all cases some form of programmable address generation. The principles and techniques explained here for the use of the PDSP1640 may be used as the basis for the implementation of address generation for many other algorithms.

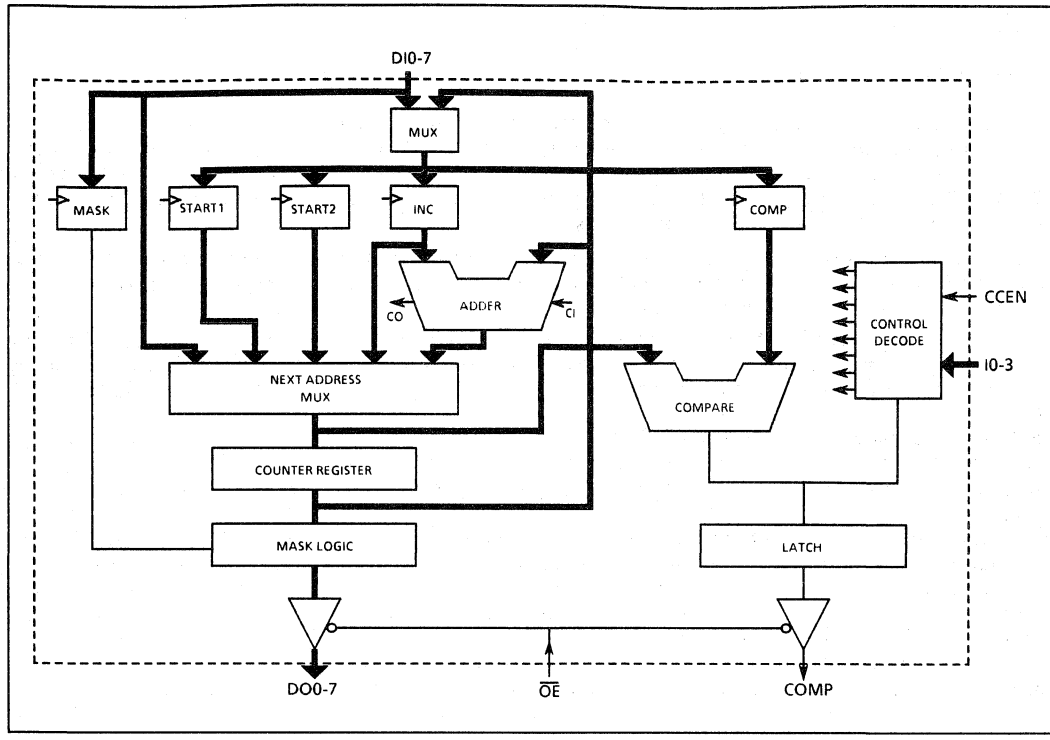


Fig 3. PDSP1640 Address Generator Block Diagram

1.2 Plessey PDSP1640 Address Generator

The Plessey PDSP1640 is an 8-bit programmable address generator capable of operating at speeds up to 40MHz (PDSP1640A). It may be cascaded with other devices to produce wider address fields, for example operating at up to 20MHz for a 24 bit address, and is ideally suited to many situations requiring high speed address generation, both for FFT computation and for other digital signal processing applications.

A block diagram of the PDSP1640 is shown in fig 3. It consists of five user programmable registers, an 8-bit address counter, a comparator and instruction decode logic, together with an output multiplexer and mask logic. The various instructions allow each of the registers to be loaded from a number of sources or for the address counter register to be incremented, via the 8-bit adder, by the value specified in the increment register. Carry in and carry out signals are available to implement the cascading of the adder with those from other devices. The increment instructions may be conditional such that if a particular address count is reached, a jump to another specified address will occur. By programming the device with a suitable sequence of instructions and data, it is possible to generate the desired address sequence.

For cascaded devices, the instructions input to each device are the same, however the data associated with these instructions will vary. For two 1640s, for example, the devices may be regarded as a single unit with the data being 16 bits wide.

2 In-Place FFT Algorithm

2.1 Data Memory Addressing

Since the data output at each stage is put back into the same memory location from which the input data is read, the write address sequence is exactly the same as the read address sequence, but delayed by the numbr of clock cycles required to execute the FFT butterfly. Using the Plessey PDSP16112 complex multiplier and the PDSP16318 complex accumulator, this delay is 10 clock cycles. It is therefore possible to use a single address generator for both the read and write sequences.

Two words of data must be read from memory and two words written back again during each butterfly clock cycle, requiring the use of fast dual port RAM and some additional buffering to present the two input words to the butterfly processor at the same time.

From fig 1, it can be seen that the register address sequence for the first stage is: 0 & 1; 2 & 3; 4 & 5;....etc. This can be achieved by simply incrementing the address counter register of the PDSP1640 by one after each memory access from zero until the last data register is reached, as indicated by the COMP output from the PDSP1640.

For the second stage, the data address sequence is slightly more complicated, being 0 & 2; 1 & 3; 4 & 6; 5 & 7; 8 & 10;....etc, which is rather difficult to generate in this jumbled order. Since the order in which the butterflies are executed within each stage is not important, this sequence may be re-arranged into even and odd sequences of 0 & 2; 4 & 6; 8 & 10;....etc and 1 & 3; 5 & 7; 9 & 11;....etc. These two half length series each have an increment of two between consecutively generated addresses, which is easily achieved. The only remaining problem is to get from the end of the first series to the start of the second. One way of achieving the jump between the two series is to set the compare register to the end of the first half series (i.e. to N-2) and the START1 register to the beginning of the second (i.e. to 1). The CCJS1 instruction is then used to increment the address counter until the compare flag becomes active and a jump takes place to the location specified in the START1 register. At this point the compare register must be reloaded with the end of the second half series (N-1) and counting continued using CCJS2, the START2 register having been previously set to zero for the start of the next stage. This method is obviously rather cumbersome, particularly for subsequent stages where more than two sub-series are necessary.

An alternative method achieves the step between the series automatically, but requires some redundancy in the address bits actually used. In the 16-point FFT example, only four address bits are required. If the generated address from the 1640 is shifted to the left by three positions, such that the three least significant bits and the most significant bit are not used, the increment required at each step for each sub-series then becomes 10H (0 0010 000) instead of 02H (0000 0010). After seven increments of 10H, an increment of 18H is necessary, which causes the address counter to jump from address 70H to 88H (or 08H as MSB is not used, i.e. from 0 1110 000 to X 0001 000). This may be achieved by specifying an actual increment for each step of 11H, which will produce the 16 step count sequence shown in fig 4a. The unused bits of the output address may be masked off by use of the mask register.

	ADDRESS SEQUENCE	COUNT SEQUENCE
INCREMENT = 11H	0	0 (0000) 000
	2	0 (0010) 001
	4	0 (0100) 010
	6	0 (0110) 011
	8	0 (1000) 100
	10	0 (1010) 101
	12	0 (1100) 110
	14	0 (1110) 111
	1	1 (0001) 000
	3	1 (0011) 001
	5	1 (0101) 010
	7	1 (0111) 011
	9	1 (1001) 100
	11	1 (1011) 101
	13	1 (1101) 110
	15	1 (1111) 111

a

	ADDRESS SEQUENCE	COUNT SEQUENCE
INCREMENT = 22H	0	0 (0000) 000
	4	0 (0100) 010
	8	0 (1000) 100
	12	0 (1100) 110
	1	1 (0001) 000
	5	1 (0101) 010
	9	1 (1001) 100
	13	1 (1101) 110
	2	0 (0010) 000
	6	0 (0110) 010
	10	0 (1010) 100
	14	0 (1110) 110
	3	1 (0011) 000
	7	1 (0111) 010
	11	1 (1011) 100
	15	1 (1111) 110

b

Fig 4. PDSP1640 Address Count Sequence using Bit Redundancy

A similar technique may be used for subsequent stages. The third stage, for example, requires registers to be addressed in the sequence 0 & 4; 8 & 12 then 1 & 5; 9 & 13 and so on. By specifying an increment at each step of 22H, the count sequence of fig 4b is produced.

By cascading PDSP1640 devices together, this technique may be extended to any size of FFT. For the general case, the number of redundant least significant bits required for an N-point FFT is $(\log_2 N - 1)$. The increment at each stage of the FFT is given by:

$$\text{Increment, } i = 2^{(m-2)}(N + 1),$$

where m (= 1,2,3....$\log_2 N$) is the number of the stage of the FFT. The fractional part of the result for the first stage may be ignored.

For the 16-point FFT of fig 1, the instruction sequence for the whole FFT is shown in table 1. It consists of initialising the counter register and the START1 register to address 00H, loading an initial increment for the first stage of 08H into the increment register and setting the compare register to the final address required for the first stage (78H). The mask register is optionally loaded to mask off the unused address bits and counting started. At the end of each stage, the increment register is simply loaded with the new increment value and the compare register with the final address of the next stage. This technique enables each stage to be executed without a break in the sequence of addresses generated.

CYCLE NO.	MNEMONIC	OP. CODE	DATA[1,2]	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LIRDI	CH	XX	LOAD INCREMENT REGISTER
3	LCPDI	EH	08	LOAD COMPARE REG. WITH END ADDR
4	LS1DI	8H	78	LOAD START1 REG. WITH BRANCH ADDRESS
5	LMRDI	3H	00	LOAD MASK REGISTER
6	CCJS1	1H	87	COUNT BY INC OR GO TO SR1
7	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
21	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
22	LIRDI	CH	XX	LOAD INCREMENT REGISTER
23	LCPDI	EH	11	LOAD COMPARE REG. WITH END ADDR
24	CCJS1	1H	FF	COUNT BY INC OR GO TO SR1
25	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
39	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
40	LIRDI	CH	XX	LOAD INCREMENT REGISTER
41	LCPDI	EH	22	LOAD COMPARE REG. WITH END ADDR
42	CCJS1	1H	FE	COUNT BY INC OR GO TO SR1
43	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
57	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
58	LIRDI	CH	XX	LOAD INCREMENT REGISTER
59	LCPDI	EH	44	LOAD COMPARE REG. WITH END ADDR
60	CCJS1	1H	FC	COUNT BY INC OR GO TO SR1
61	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
75	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1

Table 1 Data Addressing Instruction Sequence for In-Place Algorithm

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

2.2 Coefficient Addressing

The simplest way of achieving the sequence of coefficients is to program a PROM with the correct sequence as required by the complete algorithm. The address generator is then simply programmed to count up to the maximum number of coefficients used. This, however, is a very inefficient method in terms of memory usage since each coefficient occurs several times. An alternative method requires each coefficient to be stored only once and makes use of the output masking capability of the PDSP1640.

The coefficients are held in PROM in numerical order (i.e. W^0, W^1, W^2,....$W^{(N/2-1)}$) and the PDSP1640 programmed to cycle through all coefficient addresses during each stage of the FFT algorithm. This means that the address sequence generated by the counter register is the same for all stages. By considering the required coefficients for each stage and the order in which the FFT butterflies are executed, it is possible to utilise the mask register to select a sub-set of the generated addresses. For the first stage, only W^0 is required. This can easily be achieved by loading the mask register with all 1's, which freezes all outputs and produces address 00H for each cycle. For the second stage, W^0 and W^4 are required in the order W^0, W^0, W^0, W^0, W^4, W^4, W^4, W^4, to match the order of execution of the butterflies. If the mask register is loaded with the data FBH, only bit 2 is enabled whilst all the others are frozen at logic 0. This has the effect of producing the address 00H for half of the sequence and 04H for the other half at the device outputs. Similarly for the third stage, F9H is loaded into the mask register and F8H for the last stage. Table 2 shows the complete instruction sequence for generating the coefficient addresses. It should be noted that only one instruction is required between stages for the coefficient addressing whereas two were required for the data addressing. Since the coefficient address generator runs at half the clock speed of the data address generator, the two count sequences remain in step.

CYCLE NO.	MNEMONIC	OP. CODE	DATA[1,2]	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LIRDI	CH	XX	LOAD INCREMENT REGISTER
3	LCPDI	EH	01	LOAD COMPARE REG. WITH END ADDR
4	LS1DI	8H	07	LOAD START1 REG. WITH BRANCH ADDRESS
5	LMRDI	3H	00	LOAD MASK REGISTER
6	CCJS1	1H	FF	COUNT BY INC OR GO TO SR1
7	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
13	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
14	LMRDI	3H	XX	LOAD MASK REGISTER
15	CCJS1	1H	FB	COUNT BY INC OR GO TO SR1
16	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
22	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
23	LMRDI	3H	XX	LOAD MASK REGISTER
24	CCJS1	1H	F9	COUNT BY INC OR GO TO SR1
25	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
31	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
32	LMRDI	3H	XX	LOAD MASK REGISTER
33	CCJS1	1H	F8	COUNT BY INC OR GO TO SR1
34	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
40	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1

Table 2 Coefficient Addressing Instruction Sequence for In-Place Algorithm

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

3 Constant Geometry Algorithm

3.1 Data Memory Addressing

The memory for this algorithm may be configured into two blocks, one for reading data and one for writing data, which swap roles at the end of each stage of the FFT. Each memory block may be further sub-divided into four quadrants, each quadrant being a separate 32-bit wide block of RAM with separate input and output ports. The two left hand quadrants are configured to accommodate data points with even valued addresses, the right hand quadrants accommodating data points with odd valued addresses. The upper two quadrants accommodate data points with address values greater than ($N/2$-1), where N is the transform size, the lower two quadrants accommodate data points with address values less than or equal to ($N/2$-1). A full discussion of this memory configuration is given in Application Note AN50 - A Fast FFT Processor using the PDSP16000 Family.

The same location address can then be supplied to each quadrant of a block, the appropriate quadrants being enabled or disabled in pairs according to the above rules. For the16 point FFT example of fig 2, the read address sequence is 0, 0, 1, 1, 2, 2, 3, 3, which accesses data points in the order 0 & 8; 1 & 9; 2 & 10; 3 & 11; ....etc, and the write address sequence is 0, 1, 2, 3, 0, 1, 2, 3, which stores data in the order 0 & 1; 2 & 3; 4 & 5;....etc. The storage of data points within each quadrant is shown diagrammatically in fig 6. Although the read and write address sequences in themselves are easy to generate, the situation is complicated by the fact that the read and write cycles alternate for each block. If dual port RAM devices are used, this presents no problem, however when using devices with single address buses, each cycle must be carefully controlled to maintain the correct timing with respect to the flow of data through the butterfly processor. For example, after a read cycle, the write cycle for either block must be delayed by a time equivalent to two processor pipeline delays to allow for the other block to complete writing data from the previous stage before reading data for the current stage. Address generators for this configuration may be allocated either one for write addresses and one for read addresses, or one address generator per block of memory, each generating read and write sequences.

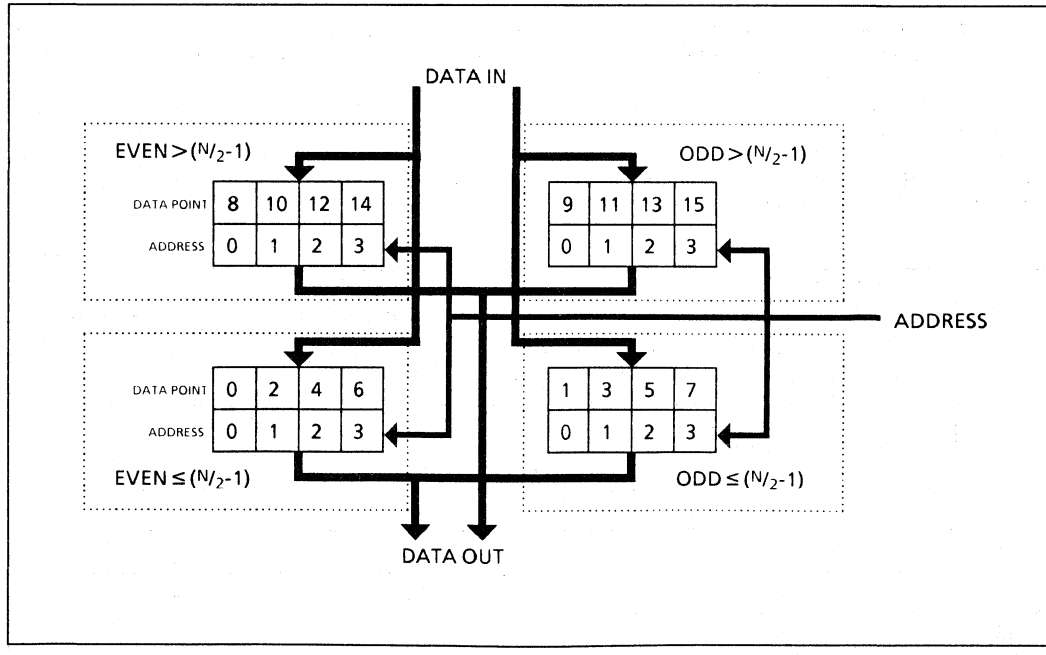


Fig 6. Data Storage for Constant Geometry Algorithm

An alternative method if dual-port RAM devices are used allows the use of a single address generator for both read and write blocks of memory. The address generator is programmed to count from 0 to ($N/2$-1) for each stage. The write addresses are taken from the least significant output bits (i.e. not using the MSB of the address) whereas the read addresses are shifted one place to the left (i.e. not using the LSB) and thus increment at half the rate of the write addresses. The write addresses would, of course, have to be delayed by the pipeline delay of the butterfly processor before being presented to the memory devices.

For the 16 point constant geometry example of Fig 2 and using dual port RAM with a single PDSP1640, the instruction sequence to program the device is shown in table 3. Although no new instructions are required between stages, one dummy instruction may be required to keep the data address generation in step with the coefficient addressing.

CYCLE NO.	MNEMONIC	OP. CODE	DATA[1,2]	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LIRDI	CH	XX	LOAD INCREMENT REGISTER
3	LCPDI	EH	01	LOAD COMPARE REG. WITH END ADDR
4	LS1DI	8H	07	LOAD START1 REG. WITH BRANCH ADDRESS
5	CCJS1	1H	00	COUNT BY INC OR GO TO SR1
6	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
(36)	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1

Table 3 Data Addressing Instruction Sequence, Constant Geometry Algorithm

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

3.2 Coefficient Addressing

From fig 2 it may be seen that the coefficient addressing sequence for each stage is in fact a count from 0 to ($N/2$-1) in bit reversed order, or a repeated sub-set of it. The sequence for each stage may be generated by programming the 1640 to count through the full address sequence and at each stage masking different output bits. The address generator outputs are then wired in bit reversed order to a PROM holding each of the coefficient terms. For the first stage all outputs are masked, thus producing an address of zero for all cycles. For the second stage, the least significant bit is unmasked; for the third stage the two least significant bits are unmasked and so on, producing the output address sequence shown in table 4. The instruction sequence to generate these addresses is as shown in table 5.

ADDR CNTR REG.	1ST STAGE MASK = FFH		2ND STAGE MASK = FEH		3RD STAGE MASK = FCH		4TH STAGE MASK = F8H	
	OUTPUT ADDR	BIT RVRSD ADDR	OUTPUT ADDR	BIT RVRSD ADDR	OUTPUT ADDR	BIT RVRSD ADDR	OUTPUT ADDR	BIT RVRSD ADDR
00	00	00	00	00	00	00	00	00
01	00	00	01	80	01	80	01	80
02	00	00	00	00	02	40	02	40
03	00	00	01	80	03	C0	03	C0
04	00	00	00	00	00	00	04	20
05	00	00	01	80	01	80	05	A0
06	00	00	00	00	02	40	06	60
07	00	00	01	80	03	C0	07	E0

Table 4 Coefficient Output Address Sequence for Constant Geometry Algorithm

CYCLE NO.	MNEMONIC	OP. CODE	DATA[1,2]	OPERATION
1	CLRCR	7H	XX	CLEAR COUNT/MASK REGISTERS
2	LIRDI	CH	XX	LOAD INCREMENT REGISTER
3	LCPDI	EH	01	LOAD COMPARE REG. WITH END ADDR
4	LS1DI	8H	07	LOAD START1 REG. WITH BRANCH ADDRESS
5	LMRDI	3H	00	LOAD MASK REGISTER
6	CCJS1	1H	FF	COUNT BY INC OR GO TO SR1
7	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
13	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
14	LMRDI	3H	XX	LOAD MASK REGISTER
15	CCJS1	1H	FE	COUNT BY INC OR GO TO SR1
16	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
22	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
23	LMRDI	3H	XX	LOAD MASK REGISTER
24	CCJS1	1H	FC	COUNT BY INC OR GO TO SR1
25	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
31	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
32	LMRDI	3H	XX	LOAD MASK REGISTER
33	CCJS1	1H	F8	COUNT BY INC OR GO TO SR1
34	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1
|				
40	CCJS1	1H	XX	COUNT BY INC OR GO TO SR1

Table 5 Coefficient Addressing Instruction Sequence, Constant Geometry Algorithm

Notes-

1. XX = don't care

2. Data is input on cycle following relevant instruction

2-D EDGE DETECTOR BOARD AP16401

The AP16401 is a real time two dimensional edge detector module for generating edge presence, magnitude and direction information from 8 bit digitized video.

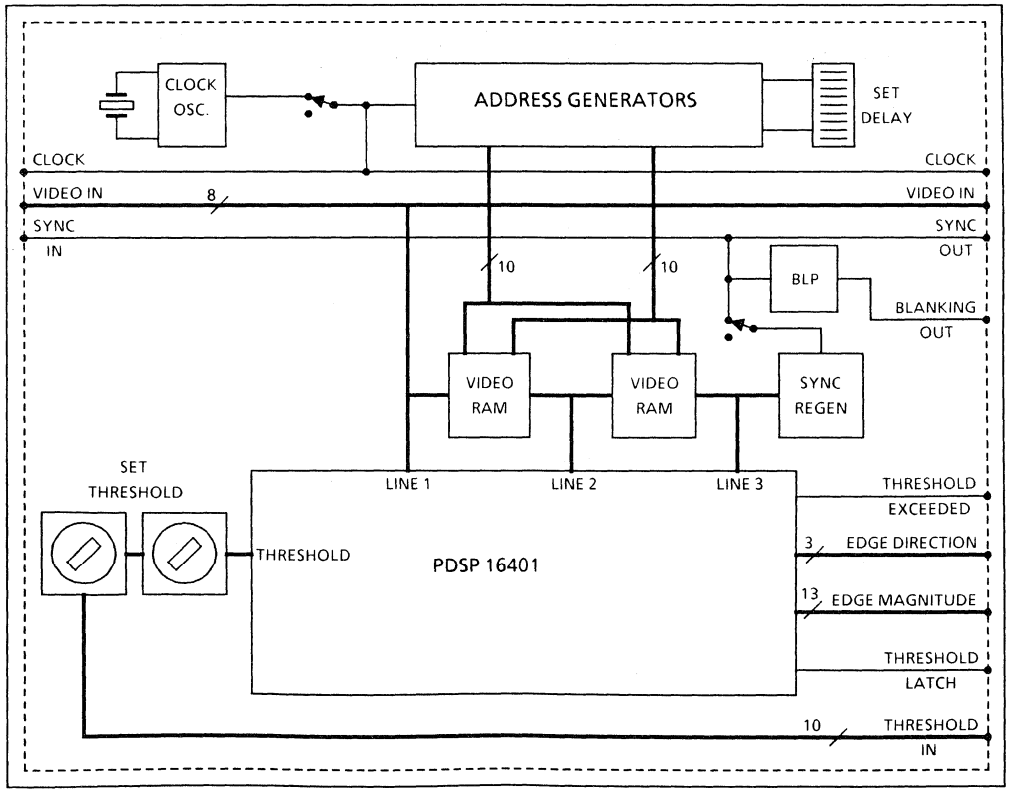
Constructed on a single Eurocard, the module incorporates a PDSP16401 2-D Edge Detector with two dual port RAMS and all necessary address generation and support logic. Sync regeneration facilities are provided to maximise video dynamic range, and a blanking pulse output is provided to allow for easy reconstruction of a composite video signal. A 10MHz crystal controlled clock is provided, though external clocks up to 15MHz may be used.

FEATURES

- PDSP16401 edge detector chip
- Two line stores
- Programmable line store delay
- Sync recovery circuit
- Black level period circuit
- On board or external threshold setting
- Single eurocard format
- 5V power supply
- External clock up to 15MHz

APPLICATIONS

- Robotic vision systems
- Pattern recognition
- Video effects generation
- Video bandwidth compression



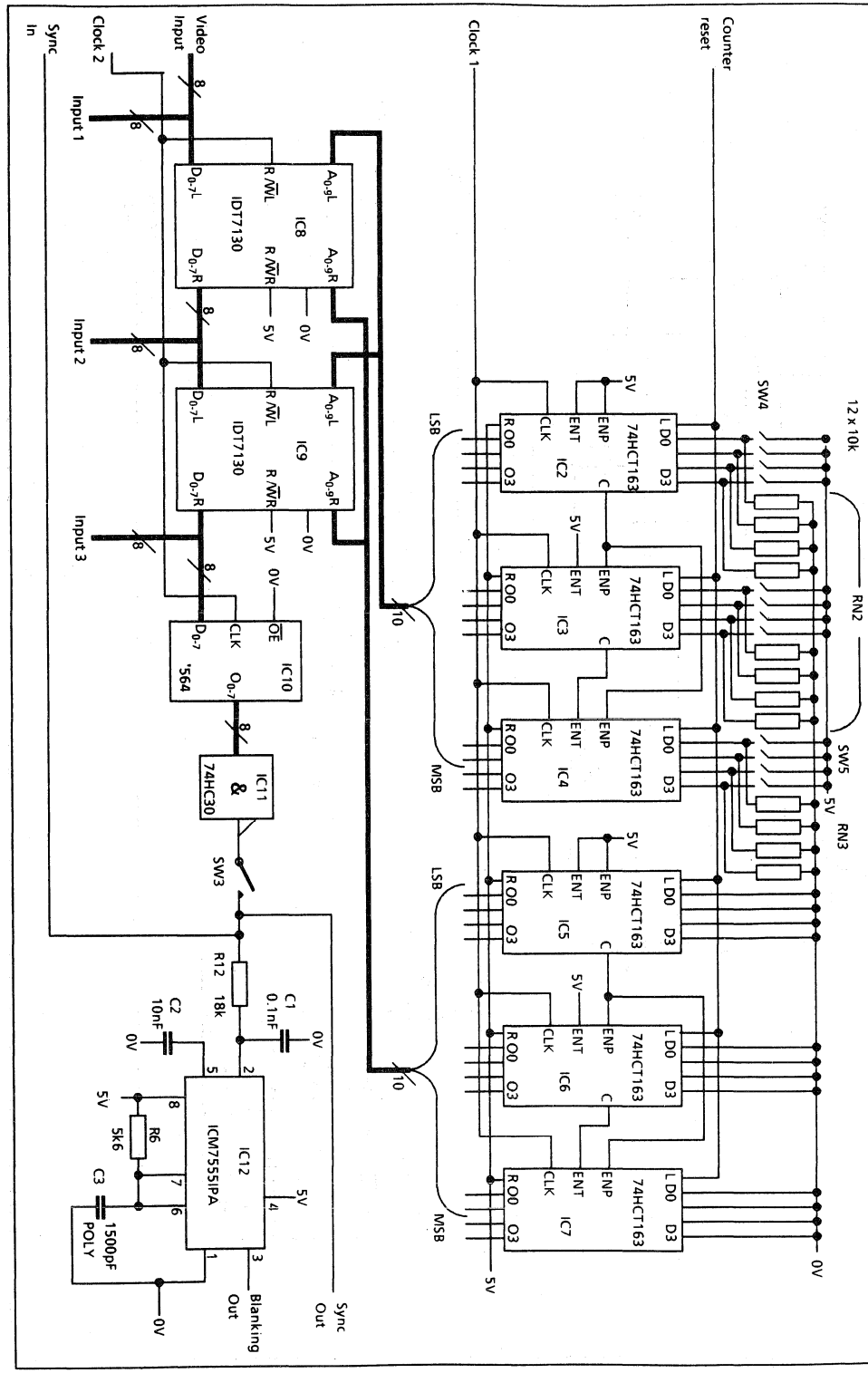


Fig. 1 Delay Lines & Sync Recovery

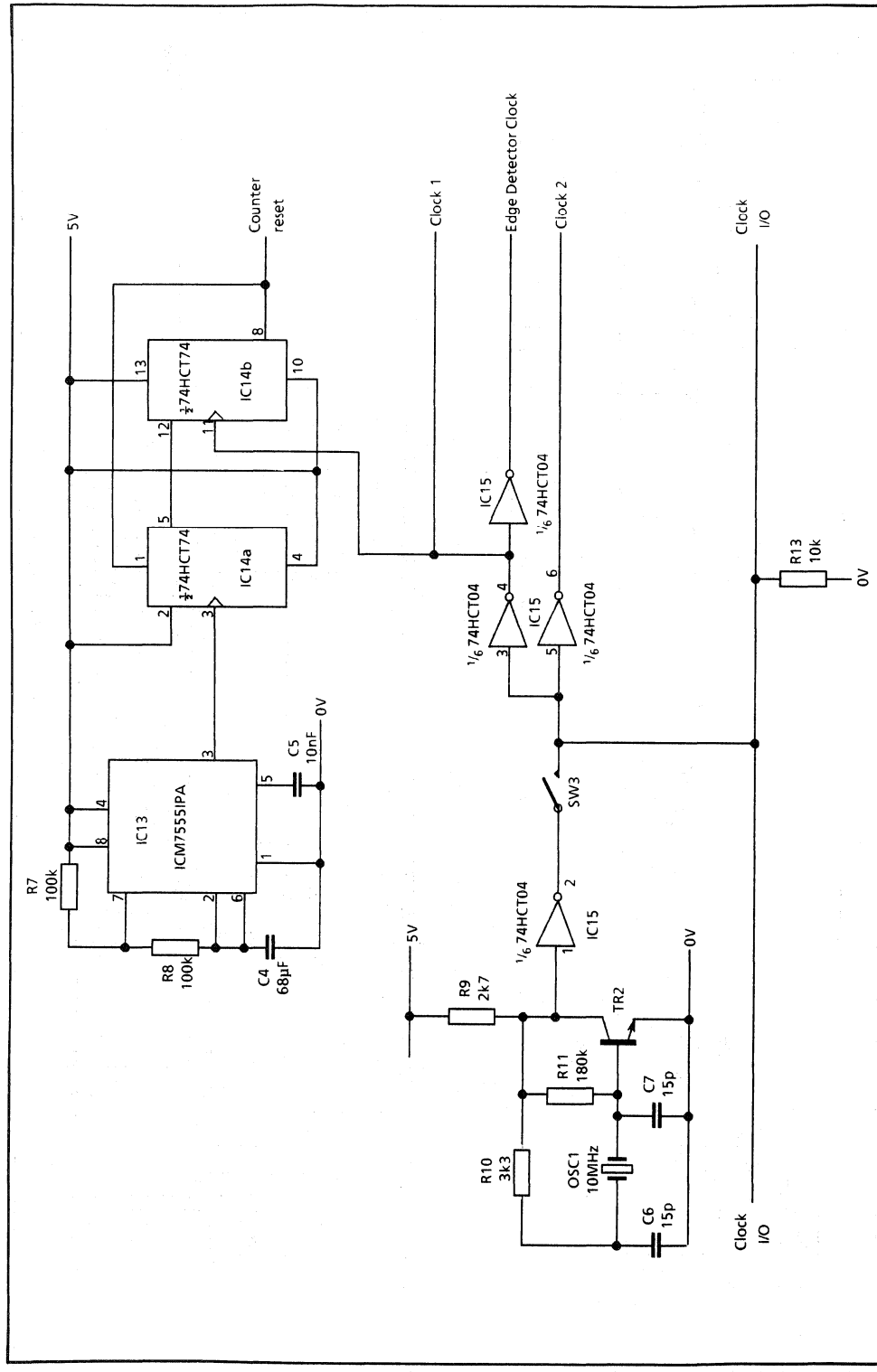


Fig. 2 Clock & counter reset circuits

REAR (DIN41612) CONNECTOR

EDGE DIRECTION OUT

	EDG1	EDG2	EDG3
Pin	29b/c	30a	30b/c

VIDEO INPUT

Bit	7	6	5	4
Pin	23a	24a	25a	26a
Bit	3	2	1	0
Pin	23b/c	24b/c	25b/c	26b/c

The data on this input must be valid on the rising edge of the clock.

EDGE MAGNITUDE OUT

Bit	12	11	10	9	8	7	6
Pin	19a	20a	20b/c	21b/c	22b/c	15b/c	16b/c
Bit	5	4	3	2	1	0	-
Pin	17b/c	13a	21a	16a	13b/c	11a	-

THRESHOLD INPUT

Bit	9	8	7	6	5
Pin	19b/c	18b/c	12a	9b/c	12b/c
Bit	4	3	2	1	0
Pin	8b/c	11b/c	6b/c	10b/c	7b/c

Note that if the threshold inputs are used, the rotary switches SW1 and SW2 **must** both be set to zero.

SYNC OUT
6a

BLACK LEVEL PERIOD (blanking)
4b/c

THRESHOLD LATCH
14a
This is pulled high on the board by a 10kΩ resistor.

THRESHOLD EXCEEDED
14b/c

CLOCK I/O
5b/c

FRONT EDGE CONNECTOR

This is a gold plated 30 way connector, with a 0.1inch contact spacing. The contacts on the underside of the board are used for signals. Pin 2 on the upper side of the board is ground. Digitised video can alternatively be input via this connector. The dual DIL switch, SW3, determines whether the clock and sync lines are inputs or outputs. SW3-1 controls the clock line and SW3-2 controls the sync line. The lines are outputs when the switches are closed.

The connections to the front of the card are:

PIN	FUNCTION	PIN	FUNCTION
1	N/C	16	D6
2	N/C	17	D7 MSB
3	N/C	18	N/C
4	N/C	19	N/C
5	N/C	20	N/C
6	N/C	21	N/C
7	N/C	22	SYNC
8	N/C	23	N/C
9	N/C	24	N/C
10	D0 LSB	25	CLOCK
11	D1	26	N/C
12	D2	27	N/C
13	D3	28	N/C
14	D4	29	N/C
15	D5	30	N/C

LINE PERIOD

The video line period is set on SW4 and SW5. The value is calculated by dividing the period of a line by the period of the 10MHz clock and subtracting 3. For example, in the UK, this value is (64µS / 0.1µS) - 3 = 637. This number is converted to binary and set on the switches. The value of each switch position together with the common settings are:

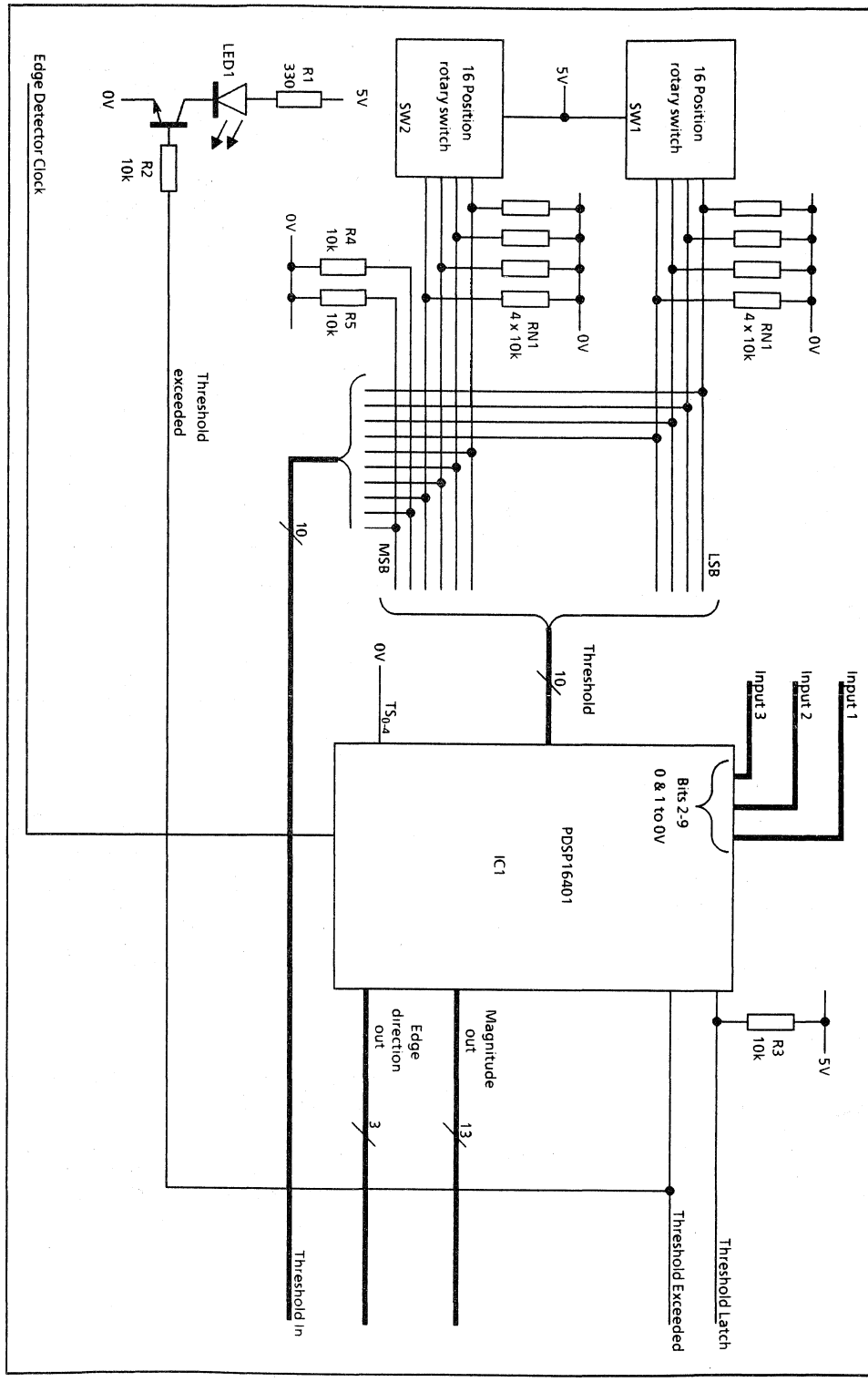


Fig. 3 PDSP16401 connections

Value	2^{11}	2^{10}	2^9	2^8	2^7	2^6
Switch	5-1	5-2	5-3	5-4	4-5	4-6
625/50Hz*	0	0	1	0	0	1
525/60Hz*	0	0	1	0	0	1
Value	2^5	2^4	2^3	2^2	2^1	2^0
Switch	4-7	4-8	4-1	4-2	4-3	4-4
625/50Hz*	1	1	1	1	0	1
525/60Hz*	1	1	1	0	0	0

* These switch settings assume normal interlacing. In this case, note that the edge detector will actually be operating on three horizontal by six vertical screen pixels, which will lose some vertical resolution.

The settings are periodically reloaded by a pulse derived from IC13 and IC14. This is done to ensure that the system will set itself up again in the event of a power supply glitch upsetting the counters.

SIGNAL INTERFACING

VIDEO

Video is input to the card in digitised form on the rising edge of the clock. The word width can be up to 8 bits. Either the front or rear edge connectors can be used. If it is desired to convert the output of the card back into composite video form, it is advantageous to digitise the video so that it is all zeros during sync pulses. This is detected by a circuit at the output of the second line store and converted back into a negative going sync pulse. This is available at the SYNC OUT pin on the rear of the card. Also available when SYNC OUT operates is the BLACK LEVEL PERIOD output. This is a positive going pulse which can be used to clamp the reconstructed composite video to black level.

THRESHOLD

The threshold is a 10 bit number which is compared with the magnitude of the current edge. If the edge magnitude exceeds the threshold then the threshold exceeded output will be active.

The threshold can be set by using the two rotary switches, or input from another card using the rear connector. On the card, the ten threshold lines are pulled low by 10kΩ resistors, with the rotary switches, which only operate on the 8 least significant bits, taking the lines to 5V. Therefore if the rear connector is used, both of the switches must be set to zero, otherwise the external device driving the card will be shorted to the 5V supply.

THRESHOLD LATCH

Threshold latch enables clocking in of the threshold data when high. It is pulled high on the card by a 10kΩ resistor. This pin is pulled low externally to fix the threshold value.

MAGNITUDE

This is a measure of the magnitude of the current edge.

THRESHOLD EXCEEDED

Either all of the data from the edge magnitude output can be used, or only data which exceed the threshold. The threshold exceeded signal indicates when this occurs and can be used, for example, to enable a gate passing the magnitude data. Alternatively, if just an outline is required, it is only necessary to use the threshold exceeded output which indicates where the edge is.

EDGE DIRECTION OUT

Each edge has a direction which takes one of eight values. These specify whether the edge is vertical, horizontal or diagonal, and which side of the edge is brighter.

CONSTRUCTING COMPOSITE VIDEO

If composite video is required, the SYNC OUT and BLACK LEVEL PERIOD outputs are used.

For example, the simplest method of displaying edges on a monitor is to use the threshold exceeded output to produce black lines on a white background, see fig. 4. To do this, THRESHOLD EXCEEDED and BLACK LEVEL PERIOD are passed through a NOR gate. A resistor network is used to add this to SYNC OUT so that the magnitude of the sync pulse is 0.66V below black and the video white level is 1.33V above black. This is buffered with a 75Ω driver for a monitor with a 75Ω input. If the monitor input is unterminated, the above voltages are halved.

Another possible video effect is to have a white background, and use the edge magnitude with a DAC to draw the edges in varying levels of grey. If the greatest magnitude edges produce the blackest lines the effect is very much like a moving pencil sketch.

CIRCUIT DESCRIPTION

The PDSP16401 requires three digitised video inputs. Inputs 2 and 3 must be delayed by one and two line periods respectively. This is implemented by the circuitry in fig. 1. IC2, IC3 and IC4 are periodically loaded with the value set on the switches SW4 and SW5, which set the time delay per line. IC5, IC6 and IC7 are loaded with all zeros. These counters operate the address inputs of the dual port RAM chips, IC8 and IC9. The left ports are written under control of the address generated by IC2, IC3 and IC4 and the right ports are read under control of the address generated by IC5, IC6 and IC7. Thus there is a delay between a byte being written into the left port of one of the RAMs and read from the right port. These two delayed video signals, along with the current video signal, are fed into the PDSP16401.

Also in fig. 1 is a digital sync detector, which operates by decoding bytes with all zeros in the digitised video. A monostable is also provided for the purpose of clamping the video for the period of the sync pulse and black level. Under some circumstances an analogue sync detector may be more successful than the the digital one. A suitable circuit is shown in fig. 5. This circuit has the advantage of also providing a DC level clamped video signal which can be input to the ADC.

Fig. 2 shows the system clock, which is a simple crystal controlled transistor oscilator with inverters to provide buffering and different phases.

The reset circuit periodically provides a pulse which reloads the original starting values into the counters. This was provided to make the system restart itself in the event of a glitch on the power supplies.

Fig. 3 shows the connections to the PDSP16401 and the method of setting the threshold input, which can be done using either the rotary switches or the edge connector. The LED is provided to give an indication of the activity of the threshold exceeded output.

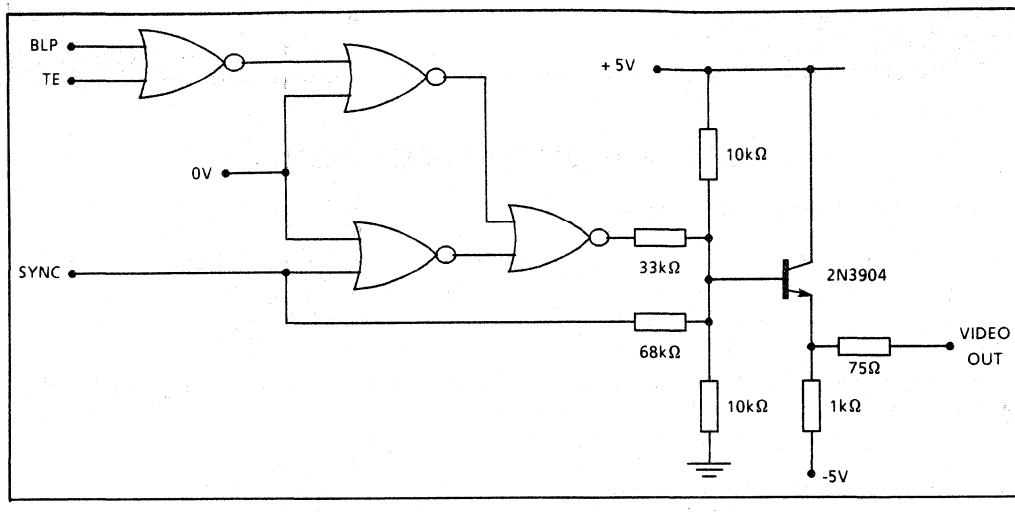


Fig. 4 Example circuit to produce composite video from threshold exceeded output

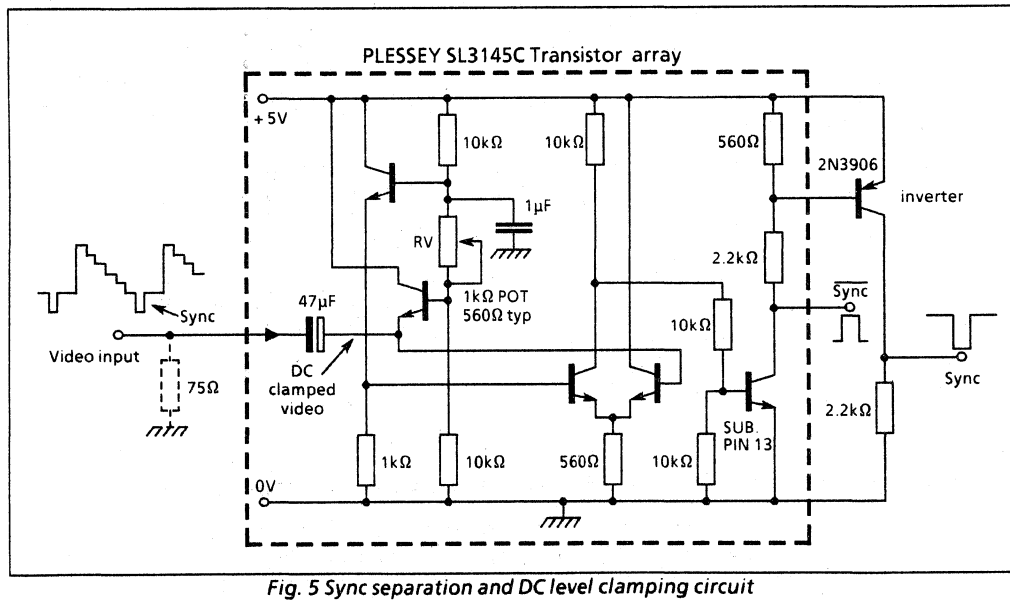


Fig. 5 Sync separation and DC level clamping circuit

SOBEL v. PDSP16401 OPERATORS

The Sobel operator in common use is given by:

$$S(x) = \left| (x) * \begin{bmatrix} -1 & 0 & 1 \\ -1 & 0 & 1 \\ -1 & 0 & 1 \end{bmatrix} \right| + \left| (x) * \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \\ -1 & -1 & -1 \end{bmatrix} \right|$$

The four-operator system used by the PDSP16401 gives a magnitude output which is the greatest of the four convolutions of the operators below with the input array:

$$1.5 * \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \\ -1 & -1 & -1 \end{bmatrix} \qquad 1.5 * \begin{bmatrix} 1 & 0 & -1 \\ 1 & 0 & -1 \\ 1 & 0 & -1 \end{bmatrix}$$

$$\begin{bmatrix} 2 & 1 & 0 \\ 1 & 0 & -1 \\ 0 & -1 & -2 \end{bmatrix} \qquad \begin{bmatrix} 0 & -1 & -2 \\ 1 & 0 & -1 \\ 2 & 1 & 0 \end{bmatrix}$$

The characteristic of an ideal edge enhancement operator is that it gives a constant degree of enhancement irrespective of the orientation of the edge. To test this characteristic a test edge of constant gradient and variable angle is used:

$$\begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \text{(i)} \qquad \begin{bmatrix} 1 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{(ii)}$$

$$\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{(iii)} \qquad \begin{bmatrix} 0 & 1 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \text{(iv)}$$

$$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \text{(v)} \qquad \text{etc.}$$

The table below summarises the effect of the Sobel and Plessey operators on the above test edge.

Orientation	Sobel	Plessey
i	3	4.5
ii	4	4
iii	3	4.5
iv	4	4
v	3	4.5

As can be seen, the variation in output magnitude with edge orientation with the operator set from the PDSP16401 is much smaller than that experienced with the Sobel operator.

A HIGH RESOLUTION FFT PROCESSOR USING THE PDSP16116

The PDSP16116 has been designed with an integral block floating point system which can be used, in conjunction with other Plessey PDSP parts, to process FFTs with a combination of speed and accuracy previously unobtainable. All the functionality of this BFP system is contained within the PDSP parts, which are designed to interface easily to achieve a powerful FFT solution.

A PDSP16116 based butterfly processor will allow the following FFT benchmarks:

1024 point complex radix-2 transform in 517us
512 point complex radix-2 transform in 261us
256 point complex radix-2 transform in 133us

This compares favourably with the current industry standard benchmark of around 2ms for a 1024 point complex FFT, but if speed is all important for a particular application, then the Plessey PDSP16112 16x12 Complex Multiplier can double the PDSP16116 performance with up to 70dB of dynamic range.

The FFT Algorithm

The Fast Fourier Transform is essentially a computationally efficient algorithm for extracting spectral information from signal waveforms, which may be in real time or recorded form (i.e. a transformation from the time domain to the frequency domain). It is often used to dramatic effect in a growing range of applications including radar and sonar processing, speech recognition and image processing. It is no less accurate than the related Discrete Fourier Transform (DFT), but it enjoys a vastly improved performance due to the 'divide and conquer' approach of its algorithm.

There are several variations of the FFT algorithm, each with their own merits. For high throughput, hardware implemented solutions, a variant of the Radix-2 Decimation-in-Time algorithm is most suitable. The 'Constant Geometry' algorithm (Fig.1) is easier to implement whereas the 'In-Place' algorithm (Fig.2) halves the amount of memory required.

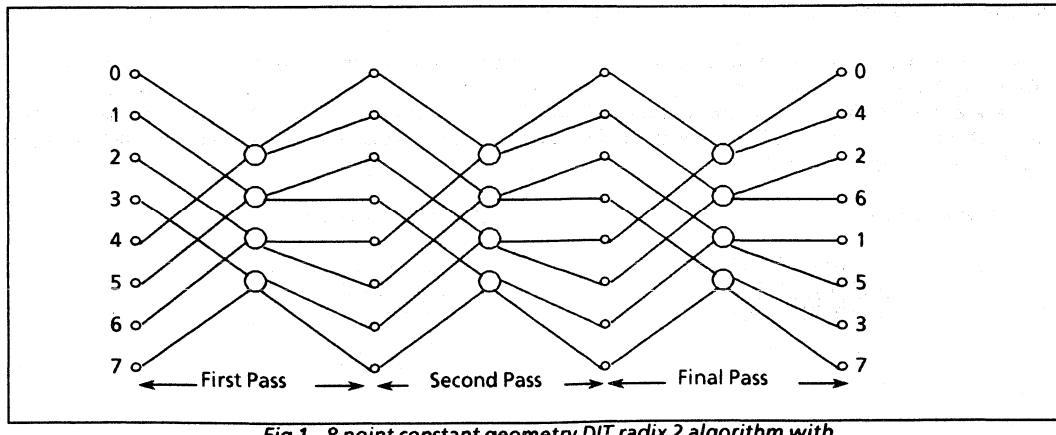


Fig 1 8 point constant geometry DIT radix 2 algorithm with normally ordered inputs and bit-reversed outputs

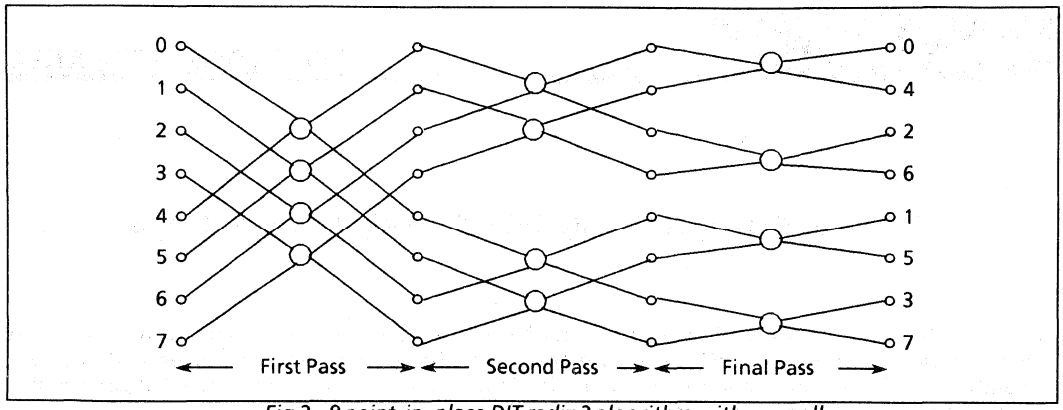
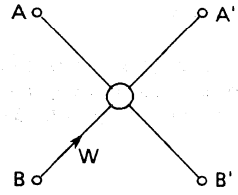


Fig 2 8 point in- place DIT radix 2 algorithm with normally ordered inputs and bit-reversed outputs

Both these variations are split vertically into a number of 'passes' ($\log_2 N$ passes for an N-point transform), each pass consisting of N/2 'butterfly' operations:



$A' = A + B.W$
$B' = A - B.W$

W is the complex coefficient and A and B are, for the first pass, the sampled data and then, in the second and subsequent passes, the values of A' and B' from the previous pass. The results of the FFT are the values of A' and B' from the butterflies of the final pass. In order to be compatible with previous FFT results, all points must be normalised to a universal format. These final complex number values (cartesian co-ordinates) may then be converted into magnitude and phase components (polar co-ordinates).

Defeating the Wordgrowth Problem

One of the most difficult problems to overcome when implementing an FFT algorithm in fixed point arithmetic is that of wordgrowth. The power of the PDSP16116's BFP system lies in its flexible and effective response to this problem. Before looking into the operation of this BFP system, the wordgrowth problem and some of the other solutions available are explained.

FFTs are implemented by means of successive multiplications and additions. Each time data is processed by an ALU (i.e. twice in each butterfly) there is the possibility of wordgrowth occuring: i.e. when two 16 bit words are added, they may produce a sum of 17 bits. The safe way to deal with this is to always pick the 16MSBs of the result. However, this will cause sign extension, i.e.repetition of the sign bit in the MSB's of the data. These two cases are illustrated in the examples below.

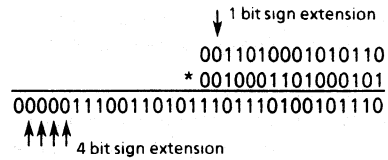
Wordgrowth occurs:

```
 0101110101110100
+0110100110101001
 01100011100011101
```

Wordgrowth does not occur:

```
 0101010111011010
+0010100010101110
 00111111010001000
 ↑
 sign extension
```

Sign extension can cause severe problems when the next multiplication occurs, as it is likely to lead to a product with a further extended sign bit. For example:



After a few passes of the FFT, there is a danger that the data could become all sign bits and no information - not much use to anyone. The common alternative to this approach is to pick the 16 LSB's from the ALU's and hope that no wordgrowth occurs, as this will then lead to overflow. If overflow is flagged during the course of an FFT, then the calculation must be aborted. The input data is then scaled down and the calculation repeated. The hit and miss nature of this approach can be avoided by automatically scaling down the inputs and accepting the resulting penalty in accuracy. A 'conditional shift' system offers some degree of flexibility. Here, the 16 LSB's are selected from the second ALU in the butterfly hardware if no overflow occurs in any butterfly during that pass.

The PDSP16116 offers a superior solution to the problem by employing an intelligent control system which can monitor data magnitudes during the course of the FFT and adjust them as necessary so as to keep extended sign bits to a minimum, whilst eliminating the possibility of overflow. In fact, this system can not only deal with wordgrowth problems as they occur, but can also adjust underscaled input data in anticipation of these problems to ensure that a valid result is obtained at the end of the calculation.

A comparison of the data formats provided by each of the methods detailed above will clarify their differences. Given input data of the format:

X.XXX... (note the position of the binary point)

The UNCONDITIONAL SHIFT implementation will output all data at the end of a pass in the format:

XXX.X...

regardless of whether the data has increased in magnitude or not.

The CONDITIONAL SHIFT implementation will either output ALL data in the format :

XX.XX...

if the maximum wordgrowth was one bit in any butterfly; or, if two bits of wordgrowth occured in any butterfly, then ALL data will be output in the format :

XXX.X...

The BFP implementation can output EACH butterfly result in ANY of the following formats, according to the data magnitude:

If data is underscaled	.XXXX...
If no worgrowth occurs	X.XXX...
If wordgrowth occurs once	XX.XX...
If wordgrowth occurs twice	XXX.X...

The adaptability of the BFP system is clearly illustrated and it is this adaptability which allows the BFP system to defeat the wordgrowth problem.

How the BFP System Operates

A block floating point system is essentially an ordinary integer arithmetic system with some additional logic, the object of which is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary weighting, i.e. the binary point should occupy the same position in every data word. This is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited.

In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point within the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point available, each denoted by a certain value of word tag:

XX.XXXXXXXXXXXXXX	word tag = 00
XXX.XXXXXXXXXXXXX	word tag = 01
XXXX.XXXXXXXXXXXX	word tag = 10
XXXXX.XXXXXXXXXXX	word tag = 11

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increases or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may change to:

XXXX.XXXXXXXXXXXX	word tag = 00
XXXXX.XXXXXXXXXXX	word tag = 01
XXXXXX.XXXXXXXXXX	word tag = 10
XXXXXXX.XXXXXXXXX	word tag = 11

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the Global Weighting Register (GWR). At the end of the final pass, the distance that the binary point has moved since the start of the FFT can be obtained by modifying the GWR according to the value of WTOUT of a particular word, as shown below:

WTOUT1:0	ADJUSTMENT TO GWR
00	SUBTRACT 1
01	NO ADJUSTMENT
10	ADD 1
11	ADD 2

For example, if the original data format was:

X.XXXXXXXXXXXXXXX

then, if the GWR = 01001 and the WTOUT = 10 for a particular word, the binary point has moved 10 places to the right of its original position and will be situated as shown below:

XXXXXXXXXXX.XXXXX

Using the GWR with Large FFT's

The Global Weighting Register represents the movement of the binary point in two's complement notation in a 5-bit field. An examination of FFT theory and the operation of the BFP system shows that, for an N-point transform, GWR will not exceed $(2 + \log_2 N)$. This means that GWR can handle transforms as large as 8K by representing the movement of the binary point as a two's complement number. However, GWR can be used for much larger transforms by noting that GWR will never drop below -8, since with this degree of left shift, the rounding noise is amplified to fill the whole 16-bit data word. This fact allows GWR to be extended and represented as a six bit value simply by ANDing the two most significant bits to produce a new sign bit (fig 3). This 6-bit field allows GWR to handle up to a 2097K transform.

Value of GWR	Decimal Equiv.	Meaning		
00000	0	Binary point has not moved		
00001	+ 1	Binary point has moved	1	place to the right
00010	+ 2		2	
00011	+ 3		3	
00100	+ 4		4	
00101	+ 5		5	
00110	+ 6		6	
00111	+ 7		7	
01000	+ 8		8	
01001	+ 9		9	
01010	+ 10		10	
01011	+ 11		11	
01100	+ 12		12	
01101	+ 13		13	
01110	+ 14		14	
01111	+ 15		15	
10000 *	+ 16		16	
10001 *	+ 17		17	
10010 *	+ 18		18	
10011 *	+ 19		19	
10100 *	+ 20		20	
10101 *	+ 21		21	
10110 *	+ 22		22	
10111 *	+ 23		23	
11000	- 8	Binary point has moved	8	places to the left
11001	- 7		7	
11010	- 6		6	
11011	- 5		5	
11100	- 4		4	
11101	- 3		3	
11110	- 2		2	
11111	- 1		1	

* not in two's complement format

Table 1 GWR values and meanings

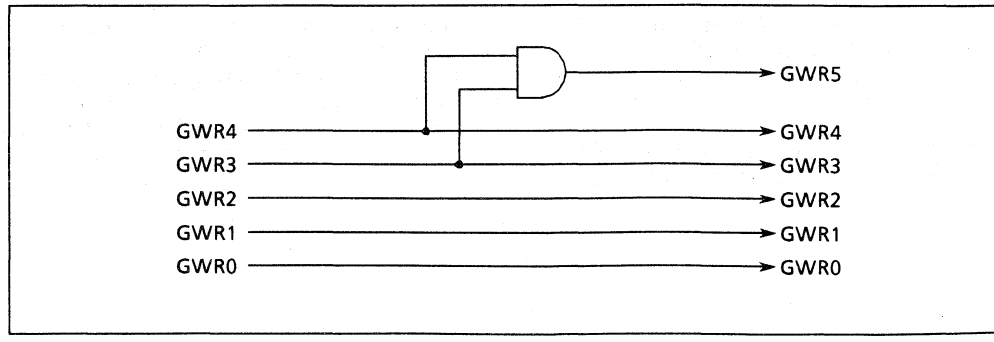


Fig 3 Extending GWR to 6 bits

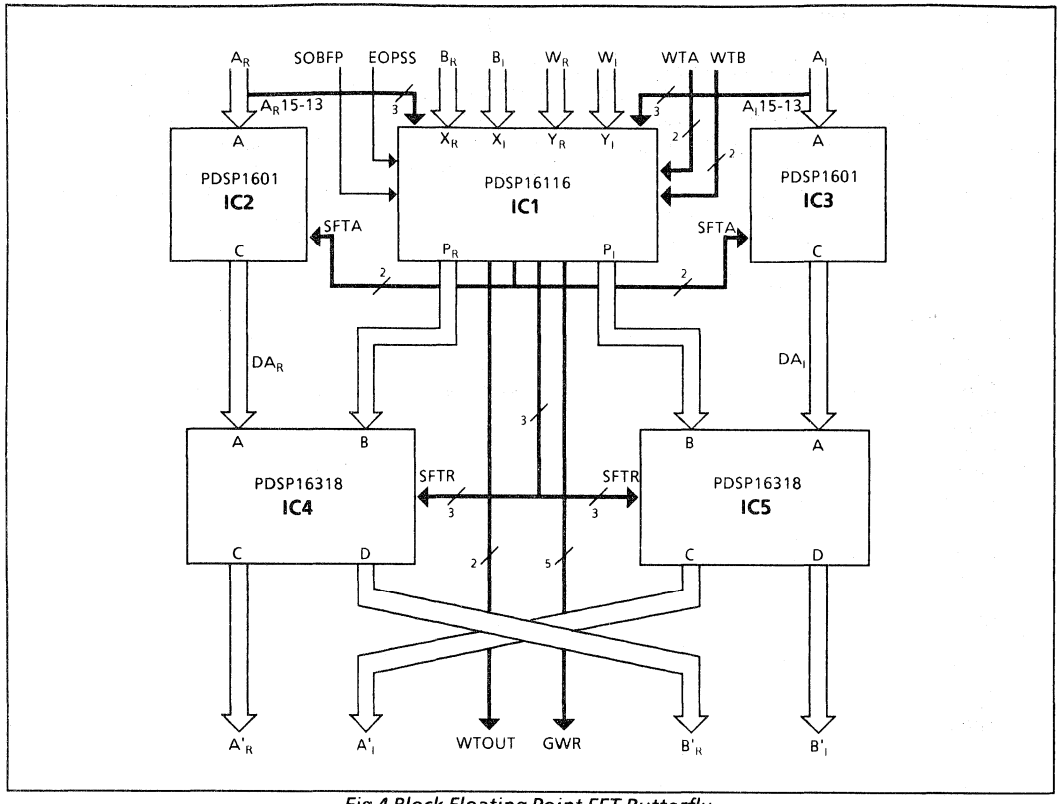


Fig 4 Block Floating Point FFT Butterfly

Construction of an FFT Butterfly Processor

As described earlier, the calculations A' = A + BW and B' = A-BW, forming a 'butterfly operation' must be carried out repeatedly in the course of an FFT. Fig.4 shows how a butterfly processor may be constructed using a single PDSP16116 in combination with two Plessey PDSP16318s and two Plessey PDSP1601s. The PDSP1601's are used to match the pipeline delay and shifting operations of the PDSP16116 to the datapath of the A word. The PDSP16318s are used to perform the complex addition and subtraction of the butterfly operation. Fig.5 details the underlying architecture of the processor.

A detailed list of the various connections required to combine these five chips into a butterfly processor appears in the Appendix. I/O connections are not specified as there are a number of I/O options that allow the butterfly processor to be interfaced with the rest of an FFT system.

A point to note is the hard-wired 1-bit right shift in the A-word data paths between the PDSP1601 outputs and the PDSP16318 inputs. This is to keep the A-word data format the same as the PDSP16116 output data format so that the two words may be added within the PDSP16318. The PDSP1601 applies a shift of 0 to 3 places to the right whereas data is output from the PDSP16116 with the binary point shifted from 1 to 4 places to the right. Hence an extra right shift of one place needs to be inserted in the PDSP1601 data path to keep the data formats compatible at the inputs to the PDSP16318 (data words must have their binary points in the same places before being added).

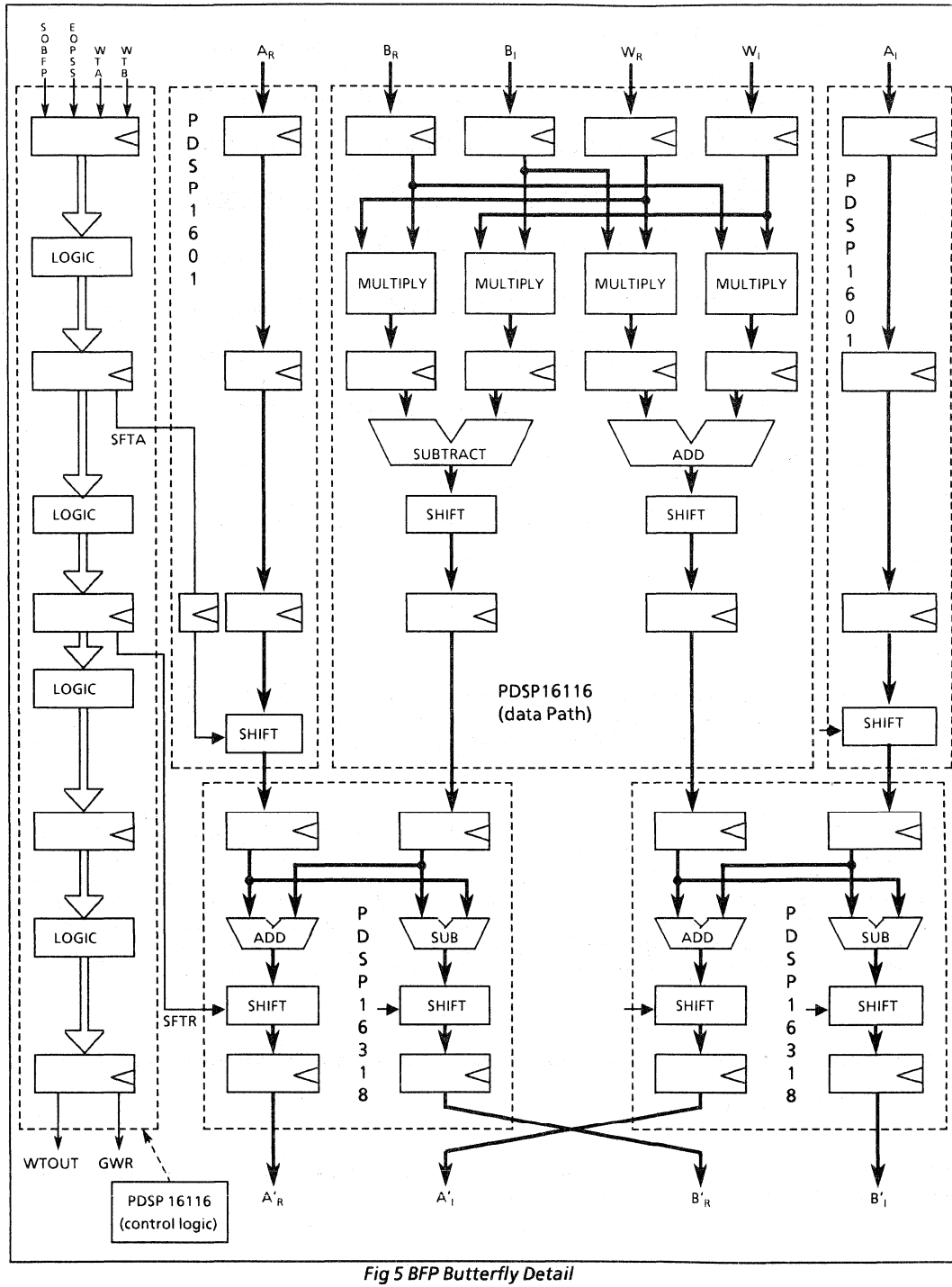


Fig 5 BFP Butterfly Detail

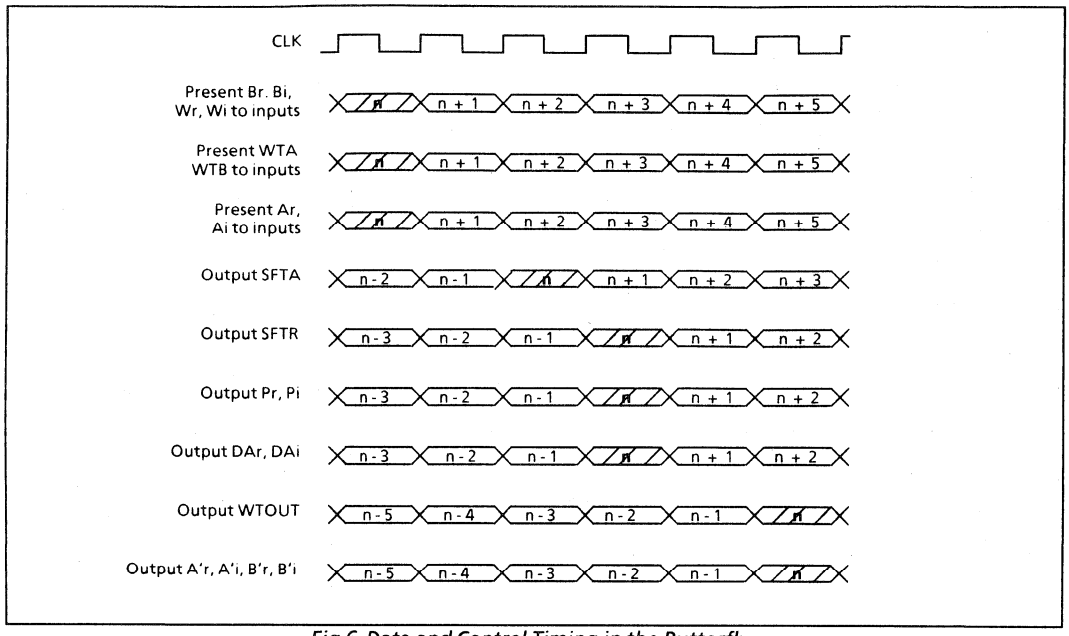


Fig 6 Data and Control Timing in the Butterfly

The Butterfly Operation

A new butterfly operation is commenced each cycle, requiring a new set of data for A, B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601 and PDSP16318. The timing of the data and control signals is shown in Fig. 6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. In every pass, each result must be stored together with its associated wordtag, WTOUT. Although WTOUT is common to both A' and B', it must be stored seperately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence the WTOUT's from one pass will become the WTA's and WTB's for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data must initially have the same weighting. Therefore, during the first pass alone, the inputs WTA and WTB are ignored.

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided:

SOBFP - start of the FFT
EOPSS - end of current pass

These inform the PDSP16116 when an FFT is starting and when each pass is complete. Fig. 7 shows the timing of these signals and an explanation of their use follows.

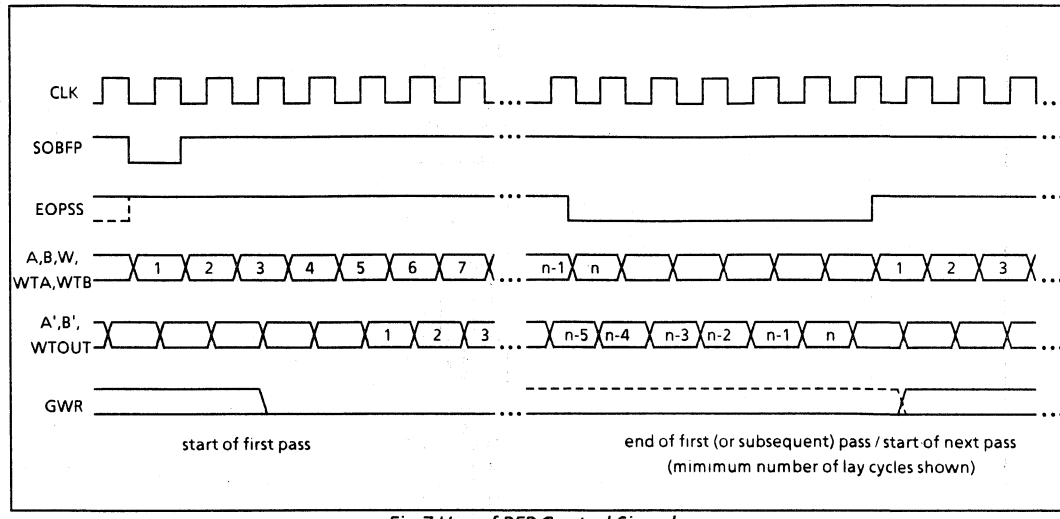


Fig 7 Use of BFP Control Signals

To commence the FFT, the signal EOPSS should be set high (where it will remain for the duration of the pass). SOBFP should be pulled low during the initial cycle, when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle, SOBFP must be pulled high where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal EOPSS should be pulled low and remain low for a minimum of five cycles, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass (should a longer pause be required between passes - to arrange the data for the next pass, for example - then EOPSS may be kept low for as long as necessary, the next pass cannot commence until it is brought high again). On the initial cycle of each new pass, the signal EOPSS should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

Building an FFT System

The Butterfly Processor is only one element of a complete FFT system. Also required are fast A/D converters at the front end of the system; a complex heterodyne filter to zoom-in on the frequencies of interest; fast memory and addressing circuits to store the data; additional fast memory and addressing circuits for the coefficients; an output normalisation circuit to make all data consistent; a Pythagoras Processor to extract magnitude and phase information from the results; finally, a D/A converter to allow the magnitude and phase information to be displayed on a video screen or oscilloscope. Fig. 8 shows how these blocks are connected. Plessey make a range of high performance DSP devices which solve the more difficult problems outlined above. The complex heterodyne filter may be constructed from a combination of either a PDSP16116 or PDSP16112 complex multiplier and either a PDSP16318 complex accumulator or two PDSP1601 augmented arithmetic logic units. The PDSP1640 is ideal for generating the data and coefficient addressing sequence. Output normalisation is a simple matter with the PDSP1601s adaptable barrel shifter and the PDSP16330 Pythagoras processor can convert cartesian to polar coordinates at 10MHz

Memory Requirements

Memory requirements differ according to whether the `In-Place' or `Constant Geometry' algorithms are used. In either case, two reads from memory (A and B) and two writes to memory (A' and B') have to be made each 100ns cycle.

For the In-Place algorithm, the results (A', B') of a butterfly are written to the same locations from which the inputs (A & B) were read. Hence, the memory must have an access time of 25ns to cope with the two reads and two writes.

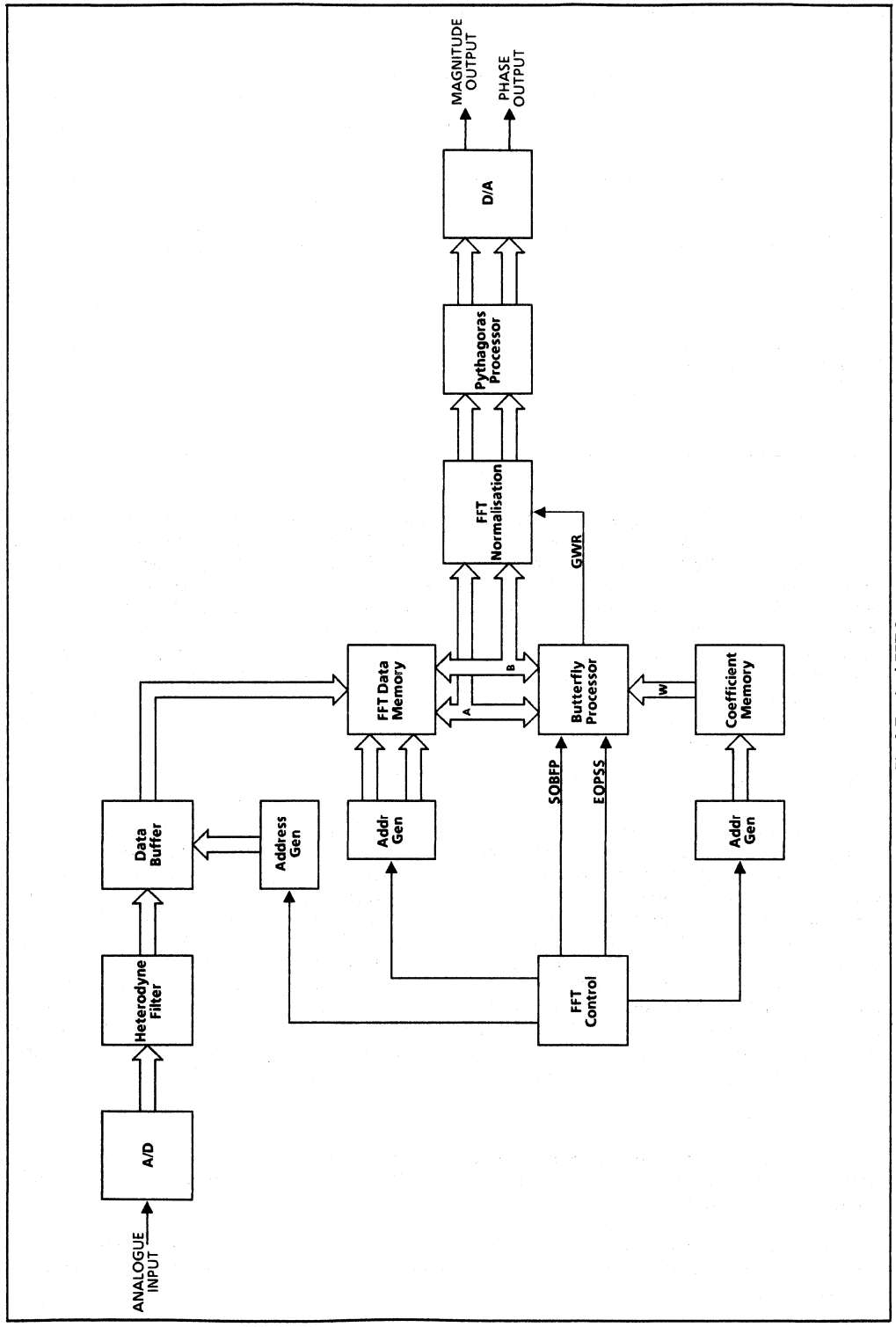


Fig 8 Typical FFT System

The Constant Geometry algorithm requires a memory access time of only 50ns, but the memory size must be double that of the In-Place algorithm. This is because the addresses written to after each butterfly are different from those from which the input data was read. This is possible due to the order in which data points are addressed.

The memory must be 32 bits wide to accommodate the real and imaginary parts of each word. Also, the 2 bit word tag must be stored with each word. This could be achieved by widening the memory to 34 bits or, alternatively, it could be stored in the LSB of the real and imaginary parts of the word, keeping the memory width at 32 bits. This would not affect the accuracy of the FFT, as the LSB is a rounded value in any case. There would be no problem in the initial pass when no word tags have been written to the memory as the PDSP16116 ignores the word tag inputs during the initial pass.

FFT Output Normalisation

In order to preserve the dynamic range of the data during the FFT calculation, the PDSP16116 employs a range of different weightings, however, at the end of the FFT, the data must be re-formatted to a pre-determined common weighting. This can be done by comparing the exponent of a given data word with the required universal exponent and then shifting the data word by the difference. The PDSP1601 Augmented ALU, with its multifunction 16-bit barrel shifter, is ideally suited to this task.

What value should the universal exponent take? Theoretically, the largest possible data result from an FFT is 1.27N times the largest input data, where N is the size of the FFT. This means that the binary point can move a maximum of $(1 + \log_2 N)$ places to the right. Hence, if the universal exponent is chosen to be $(1 + \log_2 N)$, this should give a sufficient range to represent all data points faithfully. In practice, the FFT output data may never approach the theoretical maximum, therefore it may be worthwhile trying various universal exponents and choosing the one best suited to the particular application.

Data is output from the butterfly processor with a two part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by the WTOUT value, the result being the number of places that the binary point has been shifted to the right during the course of the FFT. This value must be subtracted from the universal exponent, the difference being the shift required for that data word, which is input to the SV port of the PDSP1601.

As FFT data consists of real and imaginary parts, either two PDSP1601s must be used or a single PDSP1601 handling real and imaginary data on alternate cycles, the same shift being applied to both parts. An example of an output normalisation circuit is shown in Fig 9. Only 4-bit arithmetic is used in calculating the shift which means that very small (negative) values of GWR must be trapped and a forced 16-bit right shift applied. (N.B. It is easier to simply add the word tag value to the GWR to determine the shift rather than modifying it exactly. To compensate for this, the universal exponent should be increased by one)

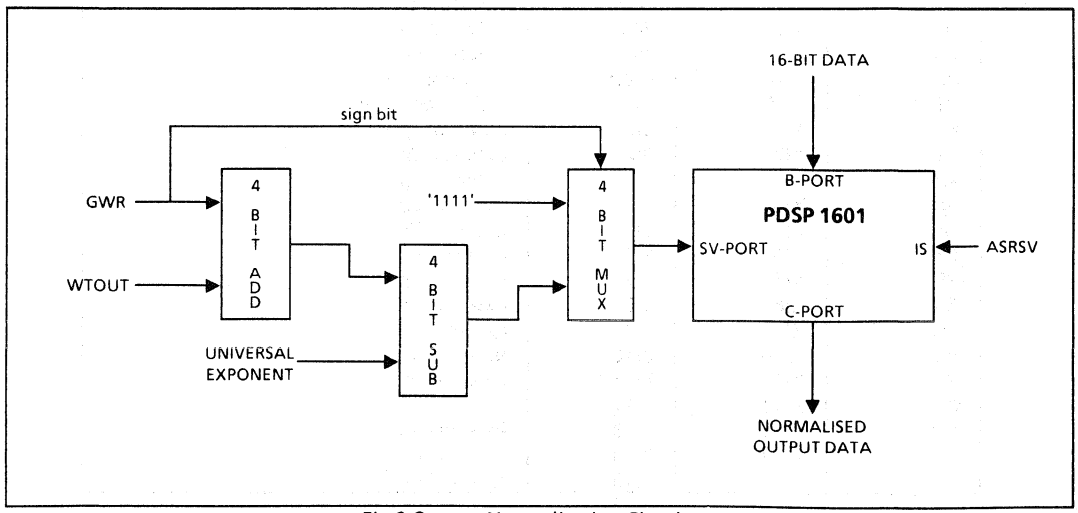


Fig 9 Output Normalisation Circuitry

Appendix A - Block Floating Point FFT Butterfly Net List

The following net lists give all the connections required for implementing the Block Floating Point FFT butterfly shown in Fig 4 of AN59:

IC 1 : PDSP16116 Complex Multiplier

Pin No.	Pin desc.	Net name	Connections
D3	PI14	PI14	IC5-C11
C2	PI15	PI15	IC5-D10
B1	WTOUT1	WTOUT1	external o/p
D2	WTOUT0	WTOUT0	external o/p
E3	SFTR0	SFTR0	IC4-L7 ; IC5-L7
C1	SFTR1	SFTR1	IC4-J7 ; IC5-J7
E2	SFTR2	SFTR2	IC4-J6 ; IC5-J6
D1	OEI		tie low
F3	CONX		tie low
F2	CONY		tie low
E1	ROUND		tie high
G2	AI13	AI13	external i/p ; IC3-H1
G3	AI14	AI14	external i/p ; IC3-F1
F1	AI15	AI15	external i/p ; IC3-G2
G1	AR13	AR13	external i/p ; IC2-H1
H2	AR14	AR14	external i/p ; IC2-F1
H1	AR15	AR15	external i/p ; IC2-G2
H3	YI15	WI15	external i/p
J3	YI14	WI14	external i/p
J1	YI13	WI13	external i/p
K1	YI12	WI12	external i/p
J2	YI11	WI11	external i/p
K2	YI10	WI10	external i/p
K3	YI9	WI9	external i/p
L1	YI8	WI8	external i/p
L2	YI7	WI7	external i/p
M1	YI6	WI6	external i/p
N1	YI5	WI5	external i/p
M2	YI4	WI4	external i/p
L3	YI3	WI3	external i/p
N2	YI2	WI2	external i/p
P1	YI1	WI1	external i/p
M3	YI0	WI0	external i/p
N3	XI0	BI0	external i/p
P2	GND	GND	0V supply rail
R1	VDD	VDD	+ 5V supply rail
N4	XI1	BI1	external i/p
P3	XI2	BI2	external i/p
R2	XI3	BI3	external i/p
P4	XI4	BI4	external i/p
N5	XI5	BI5	external i/p
R3	XI6	BI6	external i/p
P5	XI7	BI7	external i/p
R4	XI8	BI8	external i/p
N6	XI9	BI9	external i/p
P6	XI10	BI10	external i/p
R5	XI11	BI11	external i/p
P7	XI12	BI12	external i/p
N7	XI13	BI13	external i/p
R6	XI14	BI14	external i/p
R7	XI15	BI15	external i/p

IC 1 : PDSP16116 Complex Multiplier

Pin No.	Pin desc.	Net name	Connections
P8	CEY		tie low
R8	CEX		tie low
N8	XR15	BR15	external i/p
N9	XR14	BR14	external i/p
R9	XR13	BR13	external i/p
R10	XR12	BR12	external i/p
P9	XR11	BR11	external i/p
P10	XR10	BR10	external i/p
N10	XR9	BR9	external i/p
R11	XR8	BR8	external i/p
P11	XR7	BR7	external i/p
R12	XR6	BR6	external i/p
R13	XR5	BR5	external i/p
P12	XR4	BR4	external i/p
N11	XR3	BR3	external i/p
P13	XR2	BR2	external i/p
R14	XR1	BR1	external i/p
N12	XR0	BR0	external i/p
N13	YR15	WR15	external i/p
P14	YR14	WR14	external i/p
R15	YR13	WR13	external i/p
M13	GND	GND	0V supply rail
N14	VDD	VDD	+ 5V supply rail
P15	YR12	WR12	external i/p
M14	YR11	WR11	external i/p
L13	YR10	WR10	external i/p
N15	YR9	WR9	external i/p
L14	YR8	WR8	external i/p
M15	YR7	WR7	external i/p
K13	YR6	WR6	external i/p
K14	YR5	WR5	external i/p
L15	YR4	WR4	external i/p
J14	YR3	WR3	external i/p
J13	YR2	WR2	external i/p
K15	YR1	WR1	external i/p
J15	YR0	WR0	external i/p
H14	EOPSS	EOPSS	external i/p
H15	VDD	VDD	+ 5V supply rail
H13	SOBFP	SOBFP	external i/p
G13	WTB1	WTB1	external i/p
G15	WTB0	WTB0	external i/p
F15	WTA1	WTA1	external i/p
G14	WTA0	WTA0	external i/p
F14	MBFP		tie high
F13	CLK	CLK	external i/p - common to all ICs
E15	OSEL1		tie low
E14	OSEL0		tie low
D15	OER		tie low
C15	SFTA0	SFTA0	IC2-L6 ; IC3-L6
D14	SFTA1	SFTA1	IC2-L8 ; IC3-L8
E13	GWR0	GWR0	external o/p
C14	GWR1	GWR1	external o/p
B15	GWR2	GWR2	external o/p
D13	GWR3	GWR3	external o/p
C13	GWR4	GWR4	external o/p
B14	PR15	PR15	IC4-D10
A15	PR14	PR14	IC4-C11

IC 1 : PDSP16116 Complex Multiplier

Pin No.	Pin desc.	Net name	Connections
C12	VDD	VDD	+ 5V supply rail
B13	GND	GND	0V supply rail
A14	PR13	PR13	IC4-B11
B12	PR12	PR12	IC4-C10
C11	PR11	PR11	IC4-A11
A13	PR10	PR10	IC4-B10
B11	PR9	PR9	IC4-B9
A12	PR8	PR8	IC4-A10
C10	PR7	PR7	IC4-A9
B10	PR6	PR6	IC4-B8
A11	PR5	PR5	IC4-A8
B9	GND	GND	0V supply rail
C9	VDD	VDD	+ 5V supply rail
A10	PR4	PR4	IC4-B6
A9	PR3	PR3	IC4-B7
B8	PR2	PR2	IC4-A7
A8	PR1	PR1	IC4-C7
C8	PR0	PR0	IC4-C6
C7	PI0	PI0	IC5-C6
A7	PI1	PI1	IC5-C7
A6	PI2	PI2	IC5-A7
B7	PI3	PI3	IC5-B7
B6	PI4	PI4	IC5-B6
C6	VDD	VDD	+ 5V supply rail
A5	PI5	PI5	IC5-A8
B5	GND	GND	0V supply rail
A4	PI6	PI6	IC5-B8
A3	PI7	PI7	IC5-A9
B4	PI8	PI8	IC5-A10
C5	PI9	PI9	IC5-B9
B3	PI10	PI10	IC5-B10
A2	PI11	PI11	IC5-A11
C4	PI12	PI12	IC5-C10
C3	PI13	PI13	IC5-B11
B2	GND	GND	0V supply rail
A1	VDD	VDD	+ 5V supply rail

IC 2 : PDSP1601 - Real Path

Pin No.	Pin desc.	Net name	Connections
B10	VCC	VDD	+ 5V supply rail
A6	MSB		tie low
A5	MSS		tie high
B5	B15		tie low
C5	B14		tie low
A4	B13		tie low
B4	B12		tie low
A3	B11		tie low
A2	B10		tie low
B3	B9		tie low
A1	B8		tie low
B2	B7		tie low
C2	B6		tie low
B1	B5		tie low
C1	B4		tie low
D2	B3		tie low
D1	B2		tie low
E3	B1		tie low
E2	B0		tie low
E1	CEB		tie high
F2	CLK	CLK	external i/p - common to all ICs
F3	GND	GND	0V supply rail
G3	MSA0		tie high
G1	MSA1		tie low
G2	A15	AR15	external i/p ; IC1-H1
F1	A14	AR14	external i/p ; IC1-H2
H1	A13	AR13	external i/p ; IC1-G1
H2	A12	AR12	external i/p
J1	A11	AR11	external i/p
K1	A10	AR10	external i/p
J2	A9	AR9	external i/p
L1	A8	AR8	external i/p
K2	A7	AR7	external i/p
K3	A6	AR6	external i/p
L2	A5	AR5	external i/p
L3	A4	AR4	external i/p
K4	A3	AR3	external i/p
L4	A2	AR2	external i/p
J5	A1	AR1	external i/p
K5	A0	AR0	external i/p
L5	CEA		tie low
K6	MSC		tie high
K10	VCC	VDD	+ 5V supply rail
J6	IS0		tie low
J7	IS1		tie high
L7	IS2		tie low
K7	IS3		tie high
L6	SV0	SFTA0	IC1-C15
L8	SV1	SFTA1	IC1-D14
K8	SV2		tie low
L9	SV3		tie low
L10	SVOE		tie high
K9	RS0		tie high
L11	RS1		tie high
J10	RS2		tie high

IC 2 : PDSP1601 - Real Path

Pin No.	Pin desc.	Net name	Connections
K11	C0		N/C
J11	C1	DAR0	IC4-L11
H10	C2	DAR1	IC4-K10
H11	C3	DAR2	IC4-J10
F10	C4	DAR3	IC4-K11
G10	C5	DAR4	IC4-J11
G11	C6	DAR5	IC4-H10
G9	C7	DAR6	IC4-H11
F9	GND	GND	0V supply rail
F11	C8	DAR7	IC4-F10
E11	C9	DAR8	IC4-G10
E10	C10	DAR9	IC4-G11
E9	C11	DAR10	IC4-G9
D11	C12	DAR11	IC4-F9
D10	C13	DAR12	IC4-F11
C11	C14	DAR13	IC4-E11
B11	C15	DAR14:15	IC4-E9,E10
C10	OE		tie low
A11	BFP		N/C
B9	CO		N/C
A10	RA0		L on even cycles, H on odd cycles
A9	RA1		tie high
B8	RA2		tie low
A8	CI		tie low
B6	IA0		tie low
B7	IA1		tie high
A7	IA2		tie high
C7	IA3		tie low
C6	IA4		tie high

IC 3 : PDSP1601 - Imaginary Path

Pin No.	Pin desc.	Net name	Connections
B10	VCC	VDD	+ 5V supply rail
A6	MSB		tie low
A5	MSS		tie high
B5	B15		tie low
C5	B14		tie low
A4	B13		tie low
B4	B12		tie low
A3	B11		tie low
A2	B10		tie low
B3	B9		tie low
A1	B8		tie low
B2	B7		tie low
C2	B6		tie low
B1	B5		tie low
C1	B4		tie low
D2	B3		tie low
D1	B2		tie low
E3	B1		tie low
E2	B0		tie low
E1	CEB		tie high
F2	CLK	CLK	external i/p - common to all ICs
F3	GND	GND	0V supply rail
G3	MSA0		tie high
G1	MSA1		tie low
G2	A15	AI15	external i/p ; IC1-F1
F1	A14	AI14	external i/p ; IC1-G3
H1	A13	AI13	external i/p ; IC1-G2
H2	A12	AI12	external i/p
J1	A11	AI11	external i/p
K1	A10	AI10	external i/p
J2	A9	AI9	external i/p
L1	A8	AI8	external i/p
K2	A7	AI7	external i/p
K3	A6	AI6	external i/p
L2	A5	AI5	external i/p
L3	A4	AI4	external i/p
K4	A3	AI3	external i/p
L4	A2	AI2	external i/p
J5	A1	AI1	external i/p
K5	A0	AI0	external i/p
L5	CEA		tie low
K6	MSC		tie high
K10	VCC	VDD	+ 5V supply rail
J6	IS0		tie low
J7	IS1		tie high
L7	IS2		tie low
K7	IS3		tie high
L6	SV0	SFTA0	IC1-C15
L8	SV1	SFTA1	IC1-D14
K8	SV2		tie low
L9	SV3		tie low
L10	SVOE		tie high
K9	RS0		tie high
L11	RS1		tie high
J10	RS2		tie high

IC 3 : PDSP1601 - Imaginary Path

Pin No.	Pin desc.	Net name	Connections
K11	C0		N/C
J11	C1	DAI0	IC5-L11
H10	C2	DAI1	IC5-K10
H11	C3	DAI2	IC5-J10
F10	C4	DAI3	IC5-K11
G10	C5	DAI4	IC5-J11
G11	C6	DAI5	IC5-H10
G9	C7	DAI6	IC5-H11
F9	GND	GND	0V supply rail
F11	C8	DAI7	IC5-F10
E11	C9	DAI8	IC5-G10
E10	C10	DAI9	IC5-G11
E9	C11	DAI10	IC5-G9
D11	C12	DAI11	IC5-F9
D10	C13	DAI12	IC5-F11
C11	C14	DAI13	IC5-E11
B11	C15	DAI14:15	IC5-E9,E10
C10	OE		tie low
A11	BFP		N/C
B9	CO		N/C
A10	RA0		L on even cycles, H on odd cycles
A9	RA1		tie high
B8	RA2		tie low
A8	CI		tie low
B6	IA0		tie low
B7	IA1		tie high
A7	IA2		tie high
C7	IA3		tie low
C6	IA4		tie high

IC 4 : PDSP16318 - Real Path

Pin No.	Pin desc.	Net name	Connections
B2	D7	B'R7	external o/p
C2	D8	B'R8	external o/p
B1	D9	B'R9	external o/p
C1	D10	B'R10	external o/p
D2	GND	GND	0V supply rail
D1	VDD	VDD	+ 5V supply rail
E3	D11	B'R11	external o/p
E2	D12	B'R12	external o/p
E1	D13	B'R13	external o/p
F2	D14	B'R14	external o/p
F3	D15	B'R15	external o/p
G3	C15	A'R15	external o/p
G1	C14	A'R14	external o/p
G2	C13	A'R13	external o/p
F1	C12	A'R12	external o/p
H1	VDD	VDD	+ 5v supply rail
H2	GND	GND	0V supply rail
J1	C11	A'R11	external o/p
K1	C10	A'R10	external o/p
J2	C9	A'R9	external o/p
L1	C8	A'R8	external o/p
K2	C7	A'R7	external o/p
K3	C6	A'R6	external o/p
L2	C5	A'R5	external o/p
L3	C4	A'R4	external o/p
K4	C3	A'R3	external o/p
L4	C2	A'R2	external o/p
J5	C1	A'R1	external o/p
K5	C0	A'R0	external o/p
L5	OED		tie low
K6	OEC		tie low
J6	SD2	SFTR2	IC1-E2 ; IC5-J6
J7	SD1	SFTR1	IC1-C1 ; IC5-J7
L7	SD0	SFTR0	IC1-E3 ; IC5-L7
K7	MS		tie low
L6	ASI1		tie high
L8	ASI0		tie low
K8	$\overline{\text{DEL}}$		tie low
L9	$\overline{\text{CLR}}$		tie low
L10	ASR1		tie low
K9	ASR0		tie low
L11	A0	DAR0	IC2-J11
K10	A1	DAR1	IC2-H10
J10	A2	DAR2	IC2-H11
K11	A3	DAR3	IC2-F10
J11	A4	DAR4	IC2-G10
H10	A5	DAR5	IC2-G11
H11	A6	DAR6	IC2-G9
F10	A7	DAR7	IC2-F11
G10	A8	DAR8	IC2-E11
G11	A9	DAR9	IC2-E10
G9	A10	DAR10	IC2-E9
F9	A11	DAR11	IC2-D11
F11	A12	DAR12	IC2-D10
E11	A13	DAR13	IC2-C11
E10	A14	DAR14	IC2-B11
E9	A15	DAR15	IC2-B11

IC 5 : PDSP16318 - Imaginary Path

Pin No.	Pin desc.	Net name	Connections
D11	CEA		tie low
D10	B15	PI15	IC1-C2
C11	B14	PI14	IC1-D3
B11	B13	PI13	IC1-C3
C10	B12	PI12	IC1-C4
A11	B11	PI11	IC1-A2
B10	B10	PI10	IC1-B3
B9	B9	PI9	IC1-C5
A10	B8	PI8	IC1-B4
A9	B7	PI7	IC1-A3
B8	B6	PI6	IC1-A4
A8	B5	PI5	IC1-A5
B6	B4	PI4	IC1-B6
B7	B3	PI3	IC1-B7
A7	B2	PI2	IC1-A6
C7	B1	PI1	IC1-A7
C6	B0	PI0	IC1-C7
A6	CLK	CLK	external i/p - common to all ICs
A5	CEB		tie low
B5	OVR		N/C
C5	D0	B'I0	external o/p
A4	D1	B'I1	external o/p
B4	D2	B'I2	external o/p
A3	D3	B'I3	external o/p
A2	D4	B'I4	external o/p
B3	D5	B'I5	external o/p
A1	D6	B'I6	external o/p

IC 5 : PDSP16318 - Imaginary Path

Pin No.	Pin desc.	Net name	Connections
B2	D7	B'I7	external o/p
C2	D8	B'I8	external o/p
B1	D9	B'I9	external o/p
C1	D10	B'I10	external o/p
D2	GND	GND	0V supply rail
D1	VDD	VDD	+ 5V supply rail
E3	D11	B'I11	external o/p
E2	D12	B'I12	external o/p
E1	D13	B'I13	external o/p
F2	D14	B'I14	external o/p
F3	D15	B'I15	external o/p
G3	C15	A'I15	external o/p
G1	C14	A'I14	external o/p
G2	C13	A'I13	external o/p
F1	C12	A'I12	external o/p
H1	VDD	VDD	+ 5v supply rail
H2	GND	GND	0V supply rail
J1	C11	A'I11	external o/p
K1	C10	A'I10	external o/p
J2	C9	A'I9	external o/p
L1	C8	A'I8	external o/p
K2	C7	A'I7	external o/p
K3	C6	A'I6	external o/p
L2	C5	A'I5	external o/p
L3	C4	A'I4	external o/p
K4	C3	A'I3	external o/p
L4	C2	A'I2	external o/p
J5	C1	A'I1	external o/p
K5	C0	A'I0	external o/p
L5	OED		tie low
K6	OEC		tie low
J6	SD2	SFTR2	IC1-E2 ; IC4-J6
J7	SD1	SFTR1	IC1-C1 ; IC4-J7
L7	SD0	SFTR0	IC1-E3 ; IC4-L7
K7	MS		tie low
L6	ASI1		tie high
L8	ASI0		tie low
K8	$\overline{\text{DEL}}$		tie low
L9	$\overline{\text{CLR}}$		tie low
L10	ASR1		tie low
K9	ASR0		tie low
L11	A0	DAI0	IC3-J11
K10	A1	DAI1	IC3-H10
J10	A2	DAI2	IC3-H11
K11	A3	DAI3	IC3-F10
J11	A4	DAI4	IC3-G10
H10	A5	DAI5	IC3-G11
H11	A6	DAI6	IC3-G9
F10	A7	DAI7	IC3-F11
G10	A8	DAI8	IC3-E11
G11	A9	DAI9	IC3-E10
G9	A10	DAI10	IC3-E9
F9	A11	DAI11	IC3-D11
F11	A12	DAI12	IC3-D10
E11	A13	DAI13	IC3-C11
E10	A14	DAI14	IC3-B11
E9	A15	DAI15	IC3-B11

IC 4 : PDSP16318 - Real Path

Pin No.	Pin desc.	Net name	Connections
D11	CEA		tie low
D10	B15	PR15	IC1-B14
C11	B14	PR14	IC1-A15
B11	B13	PR13	IC1-A14
C10	B12	PR12	IC1-B12
A11	B11	PR11	IC1-C11
B10	B10	PR10	IC1-A13
B9	B9	PR9	IC1-B11
A10	B8	PR8	IC1-A12
A9	B7	PR7	IC1-C10
B8	B6	PR6	IC1-B10
A8	B5	PR5	IC1-A11
B6	B4	PR4	IC1-A10
B7	B3	PR3	IC1-A9
A7	B2	PR2	IC1-B8
C7	B1	PR1	IC1-A8
C6	B0	PR0	IC1-C8
A6	CLK	CLK	external i/p - common to all ICs
A5	CEB		tie low
B5	OVR		N/C
C5	D0	B'R0	external o/p
A4	D1	B'R1	external o/p
B4	D2	B'R2	external o/p
A3	D3	B'R3	external o/p
A2	D4	B'R4	external o/p
B3	D5	B'R5	external o/p
A1	D6	B'R6	external o/p

References

For a general introduction to FFT's the following texts are recommended :

1. Rabiner and Gold, 'Theory and Application of Digital Signal Processing', Prentice - Hall, 1975.

2. Oppenhiem and Shafer, 'Digital Signal Processing', Prentice - Hall, 1975

Other Plessey application notes and briefs of interest include:

AN47 'A Radix 2 Butterfly Processor'

AN49 'Complex Signal Processing with the PDSP16000 Family'

AN50 'A Fast FFT Processor Using the PDSP16000 Family'

AN54 FFT Address Generation using PDSP1640

AB01 'A 50ns Butterfly Processor'

AB10 'FIR Filtering with the PDSP16112 and PDSP16318'

In addition, many PDSP devices and applications are modelled on the 'PDSP Demonstrator' software, intended to be run on IBM - PC or compatibles.

Optimising the Accuracy of an FFT System

The two major design specifications of an FFT system are speed and accuracy. Matching the processing speeds of each of the different sections of the FFT system is a straightforward design task and optimises the design by ensuring that each piece of hardware operates at its maximum processing rate. The equivalent design task that ensures that each section of the FFT processor has the optimum dynamic range is far more complex, but may be simply determined for five example FFT processor systems described below.

LIMITS TO SYSTEM ACCURACY

Arithmetic accuracy relates directly to the achievable dynamic range of the FFT processor or its ability to discriminate low amplitude signals in the presence of large signals. There are several limiting factors to the overall system accuracy from the A to D converters through arithmetic bit widths to the FFT algorithm itself. An optimum design maintains a constant dynamic range throughout all sections of the FFT. A surprising result is that the A to D converter and the Arithmetic processor have a far greater influence over the achievable dynamic range than the stored constants used for windowing and as 'Twiddle Factors' in the FFT calculation itself.

The following optimisation criteria formed the basis for development of Plessey's PDSP family of Complex Digital Signal Processing Building Blocks, and the bit widths selected for the data and coefficient paths. Plessey offers optimum FFT implementations for five A to D converter sizes, simplifying the algorithm required to allow high speed for 8 and 10 bit systems, optimal bit widths for 12 and 14 bit systems and offering a new highly integrated solution for 16 bit systems.

FFT OPTIMISATION CRITERIA

Brigham and Cecchini (Ref.1) addressed this optimisation problem by developing a nomogram for determining the maximum bit widths required for each stage of a 1k FFT given an input A to D converter bit accuracy. The following tables are derived from this nomogram and relate to the specifications achievable with the Plessey PDSP family of complex signal processing building blocks.

The relevant sections of an FFT system that determine the dynamic range are:

1. The Input A to D Converter

The error factors contributed by the input A to D converter that limit dynamic range are quantisation, saturation and aperture jitter.

Quantisation is simply the number of bits in the A to D including sign bits; Saturation simply refers to errors caused when the input signal becomes larger than the maximum output value of the A to D converter. Aperture jitter refers to the difference between the point in time that the sample was meant to be taken, and when it actually was taken.

Assuming saturation can be avoided, and that quantisation is the selection criterion, then to maintain the dynamic range offered by the selected bit width, the maximum tolerable aperture jitter is given in Table 1.

These numbers assume a 2:1 overlap between consecutive transforms, and 50ns butterflies as offered by the PDSP 3-Chip Butterfly solution.

Overlap refers to the number of new samples written into the FFT between each FFT calculation. For an N point FFT if N new points are written into the processor between each calculation, then there is no overlap; if N/2 new points are written then there is a 2:1 overlap; N/4 then 4:1 etc.

If the overlap is increased to 4:1, then the tolerable jitter time doubles. If there is no overlap, then the tolerable aperture jitter time halves. Similarly if the butterfly time is doubled to 100ns, the tolerable jitter time doubles.

2. Number of Bits in Weighting Function Lookup Table

The weighting function applies a window to the input data to de-emphasis points at each end of the sample sequence. This operation minimises the distortions that result from the FFT's assumption that the input samples are part of a periodic signal. There are many different window functions used for different applications, all simply multiply each sample by a number whose value is related to the position of the sample within the input sequence.

The optimum number of bits in the weighting function lookup table, including the sign bit and assuming rounding, can be determined from Table 2. The limitation to dynamic range arising from this operation is caused by quantisation errors in the weighting function values which will be comparable with the A to D quantisation errors for comparable weighting function bit widths.

A to D bit width	Jitter as % of sample period	1024	FFT Size			
			512	256	128	64
			Max. tolerable aperture jitter in ns			
8	0.5 %	2.51	2.26	2.01	1.75	1.50
10	0.15 %	0.79	0.71	0.63	0.56	0.48
12	0.03 %	0.16	0.14	0.13	0.11	0.09
14	0.005 %	0.03	0.02	0.02	0.02	0.02
16	0.0025 %	0.01	0.01	0.01	0.01	0.01

Table 1

A to D bit width	Minimum weighting function bit width	Acceptable bit widths marginal additional error
8	7	(6)
10	9	(8)
12	11	(10)
14	13	(12)
16	15	(14)

Table 2

3. Number of Bits in Sin-Cos Lookup Table

The Sin-Cos lookup table is the source of the 'twiddle factors' used within the FFT calculations. Despite the fact that these values are used many times during the FFT, the required accuracy is no more stringent than that of the A to D converter even for large transforms (these numbers are derived from a nomogram for 1024 point transforms).

The optimum number of bits in the Sin-Cos lookup table, including the sign bit and assuming rounding, can be determined from Table 3.

A to D bit width	Minimum Sin-Cos lookup bit width
8	7
10	9
12	11
14	13
16	15

Table 3

4. Number of Bits in Arithmetic Section

The arithmetic section has the most profound effect upon the overall FFT accuracy, with bit width and chosen algorithm contributing to the total errors introduced and resulting limitation to dynamic range. The bit width contribution is easy to understand; more bits mean smaller errors. The algorithm differences depend upon the scheme used to allow for the inevitable word growth experienced within an FFT processor. The two schemes considered are termed Unconditional Scaling, and Conditional Scaling.

For unconditional scaling, the worst case word growth is assumed to occur during every pass of the FFT and fixed shifts are introduced to eliminate the possibility of overflow. This algorithm is easy to implement and allows very fast processors to be constructed, though as worst case word growth does not in practice always occur, the accuracy and hence dynamic range of this algorithm is reduced.

For conditional scaling, the results of each pass are examined and shifts are only used if word growth has actually occurred. This data-dependent algorithm is slower and requires more hardware to execute but offers greater dynamic range as illustrated in Table 4. The arithmetic bit widths shown include sign bits and maintain the dynamic range offered by the input A to D word width.

DYNAMIC RANGE ACHIEVED

Brigham and Cecchini used a rigorous measure of dynamic range in developing their nomogram. This measure gives the absolute worst case estimate of dynamic range, but is not directly related to the dynamic range observed from real signals in systems in practice. Equally the simple test of resolving a small signal in the presence of a large signal does not directly relate to the worst case dynamic range experience in practice. The true result lies somewhere between the two. Table 5 collects the specifications set out in the previous tables and adds the worst case dynamic range estimates as calculated by Brigham and Cecchini.

A to D bit width	Minimum arithmetic section bit width unconditional scaling	Minimum arithmetic section bit width conditional scaling
8	14	9
10	16	11
12	18	13
14	21	16
16	23	18

Table 4

A to D bit width	Weighting bit width	Sin-Cos bit width	Unconditional arithmetic bit width	Conditional arithmetic bit width	Dynamic range
8	7	7	14	9	38dB
10	9	9	16	11	50dB
12	11	11	18	13	62dB
14	13	13	21	16	74dB
16	15	15	23	18	86dB

Table 5

Table 5 shows clearly that for a given A to D converter bit width, the accuracy required for the 'twiddle factors' within the FFT is always less than the accuracy required for the arithmetic section even when conditional shift algorithms are employed.

THE PDSP FAMILY AND OPTIMUM FFTs

The PDSP Family of Complex DSP Building Blocks implements a Radix 2 DIT Butterfly using just three CMOS devices with an execution time of 50ns per butterfly. This Butterfly processor is optimised for FFTs with a 16 bit data path, and 12 bit coefficients. The optimal arithmetic format is supported by the PDSP16112A Complex Multiplier and two PDSP16318A Complex Accumulators. The Butterfly processor may be configured within Conditional or Unconditional Shift architectures, with all the shifting logic required for either algorithm contained within the PDSP16318 Complex Accumulator.

Optimum FFT configurations using this processor are:

1. 8 or 10 bit A to D based systems using Unconditional Shifting.

2. 12 or 14 bit A to D based systems using Conditional Shifting.

Systems that wish to make use of the dynamic range offered by 16 bit A to D converters require more sophisticated shifting algorithms such as Block Floating Point. This algorithm is automatically supported by another PDSP product the PDSP16116. The PDSP16116 Complex Multiplier, together with two PDSP16318 Complex Accumulators and two PDSP1601 ALUs form a five chip 100ns FFT Butterfly processor that supports block floating point arithmetic automatically allowing FFT System dynamic ranges to exceed 74dB.

EXAMPLE OF PDSP FFT DYNAMIC RANGE

The following plots (Figs. 1-7) demonstrate the actual dynamic range achieved using a Plessey PDSP16112 and PDSP16318 Butterfly processor on a 64 point complex transform using Unconditional Scaling.

The test signal was a combination of a full scale complex sinusoid (sampled such that it accumulated within a single frequency bin, see Fig.1) combined with another complex sinusoid 60dB down and sampled such that it was spread across several frequency bins (see Fig.2). The effect of using complex sinusoids is to eliminate the negative frequency components of the input signals, and hence remove the image signal from the FFT result. This test waveform is a more severe test than a simple sinusoid as both real and imaginary components of the FFT inputs are used, giving greater opportunity for word growth and error accumulation. The smaller signal is deliberately chosen to have a non-integer number of cycles within the window so that the energy will be spread to adjacent bins. Eliminating the windowing function from the calculation ensures a worst case result as the effect of this sampling is not reduced.

The plot in Fig.3 illustrates the composite input to the FFT showing both real and imaginary components of the input. This input waveform is (of course) made up from four sinusoids, but the low amplitude signals are not perceptible visually. The plot in Fig.4 illustrates the 'perfect' transform output calculated with 32 bit floating point arithmetic, and the plot in Fig.5 shows the actual transform output obtained from the PDSP FFT system. Brigham and Cecchini predict a worst case dynamic range of 50dB based on the limitation of the 16 bit data path using unconditional scaling.

The actual dynamic range observed between the two sinusoid components is 62dB with approximately 64dB between the large signal and the noise floor. This value demonstrates the difference between the two methods of estimating dynamic range. The plot in Fig.6 shows a close up view of the difference between the small signal and the noise floor with the large signal component removed. With windowing the small signal would be further separated from the noise floor as its energy would be more concentrated into one frequency bin. The final plot in Fig.7 illustrates the result achieved by a system using 16 bit arithmetic for both data and Sin-Cos values and using the same unconditional scaling. This plot is superimposed upon the result from the PDSP system that uses 12 bit coefficients and unconditional scaling. This composite plot shows clearly that no significant improvement in dynamic range is gained despite the more accurate Sin-Cos values used.

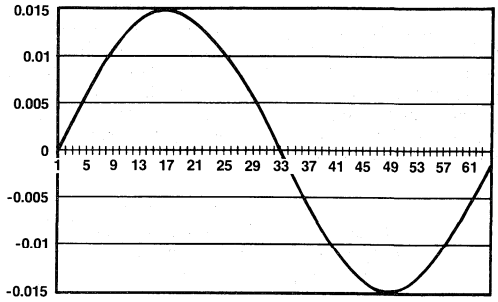


Fig.1 Imaginary portion of large input signal

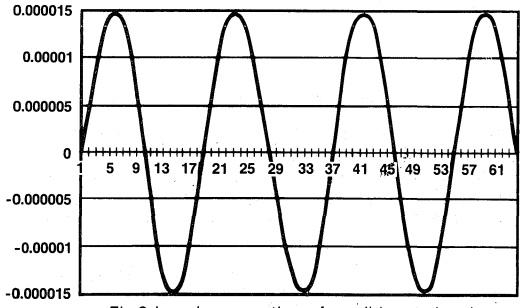


Fig.2 Imaginary portion of small input signal

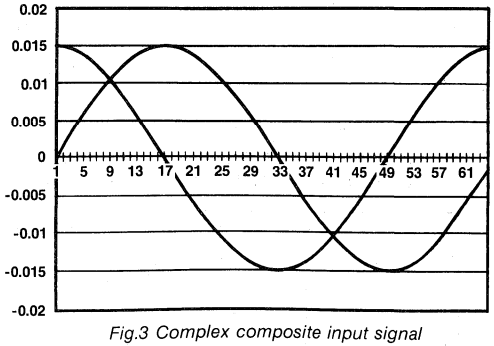


Fig.3 Complex composite input signal

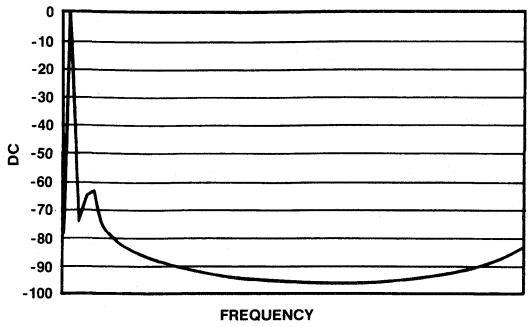


Fig.4 Perfect 64 point FFT output magnitude

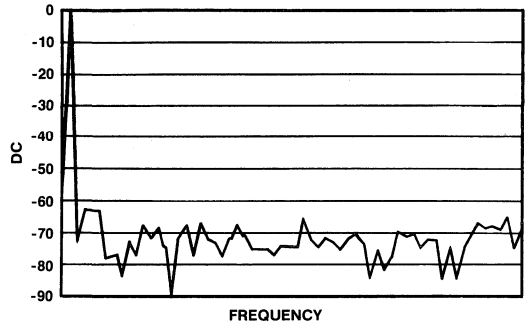


Fig.5 PDSP 64 point FFT output magnitude

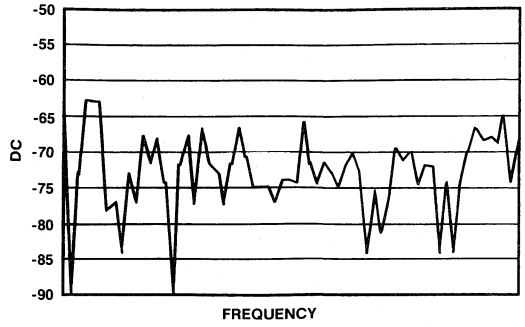


Fig.6 PDSP 64 point FFT detail of noise floor

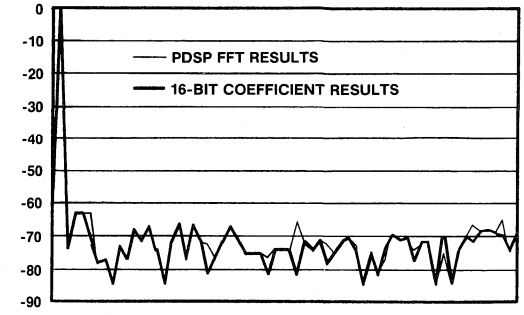


Fig.7 PDSP 64 point FFT output magnitude vs FFT using 16 bit coefficients

REFERENCES

1. A Nomogram for determing FFT system Dynamic Range - E.O. Brigham and L.R. Cecchini E-Systems, Inc. Melphar Division 7700 Arlington Blvd, Falls Church, VA 22046, U.S.A.

Support Tools

PDSP Demonstrator

The PDSP Demonstrator is a microprogram development tool for the PDSP device family offering device and system simulation facilities based upon functional models of the devices. It includes a powerful line editor for microprogram file preparation, a simulator with user control of program execution and an interactive trace facility which incorporates a print and plot function. It runs on an IBM-PC or any compatible machine under the MS-DOS operating system, the minimum configuration comprising one 360Kb floppy disc unit and 512Kb of RAM. It is therefore a convenient and powerful method of introducing the new user to the devices by 'animating' the traditional data sheet, giving a real ability to experiment with particular algorithms and speed breadboard system development.

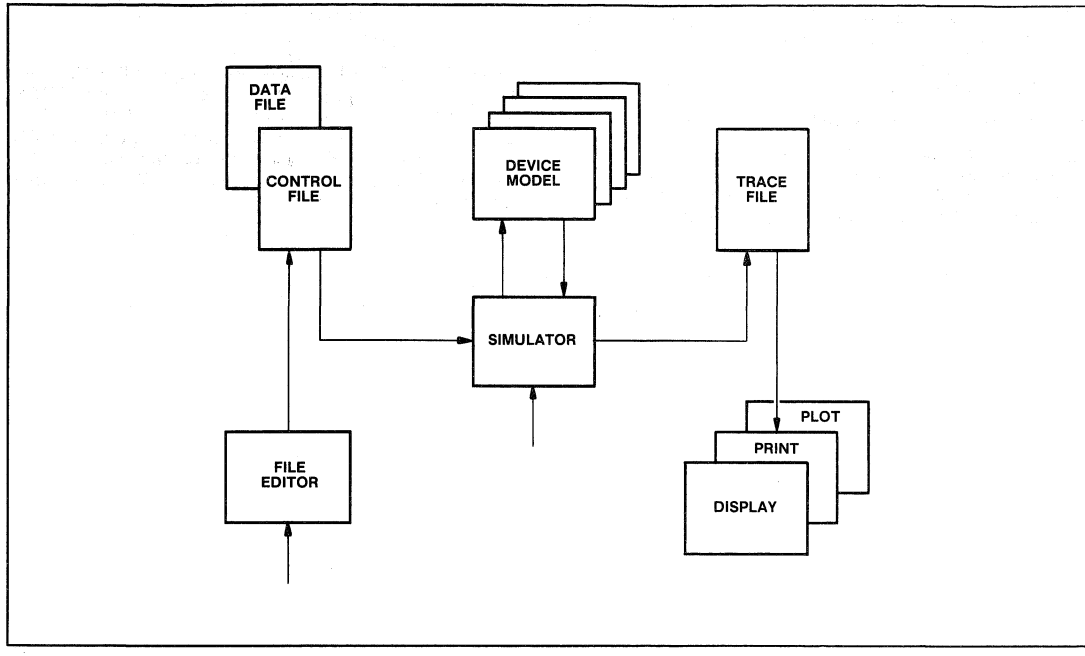


Fig.1 Demonstrator functional block diagram

FEATURES

- DSP Microprogram Development Environment
- Device/System Simulator with Programmable Breakpoint Control
- Interactive Trace Facility Including Print Function
- Graphical Representation of I/O Data
- Powerful Microprogram Editor
- High Level Program Construction using Macros
- User Friendly Interface
- Standard Application Microprogram Library
- IBM-PC Compatible Software on a Single Floppy Disc

APPLICATIONS

- Application Microcode Development
- Debugging Aid
- Test Vector Generation
- Training Aid

THE PDSP DEMONSTRATOR RANGE

The Demonstrator is available in several versions offering facilities ranging from the simulation of individual devices to the simulation of complete system solutions to common DSP problems.

The following provrams are currently available in the PDSP Demonstrator range:-

Device Function Demonstrator 1

Supports programming and simulation of the following devices:

- **PDSP1601/A** Augmented Arithmetic Logic Unit
- **PDSP1640/A** 40MHz Address Generator
- **PDSP16112/A** Complex Number Multiplier
- **PDSP16318/A** Complex Accumulator

Each model is a faithful reproduction of the real device and is programmed in accordance with its data sheet specification. All four models are programmed as individual devices only.

COMPLEX ARITHMETIC DEMONSTRATOR

Includes the same four devices as the Device Function Demonstrator 1 but supports the programming and simulation of these devices in the following system configurations:

- Dual 1640 demonstrating 16 bit addressing
- Fast Fourier Transform Processor comprised of one PDSP16112 and two PDSP16318 devices
- Complex Arithmetic Processor comprised of one PDSP16112 and one PDSP16318 device

The PDSP1601 device model is retained for programming and simulation as an individual device.

GETTING STARTED

Loading the ANSI Device Driver

The ANSI device driver is an independent software module used by the operating system to drive the display screen. It incorporates facilities for cursor movement and screen erasure which the PDSP Demonstrator requires.

To enable MS-DOS to load the ANSI device driver the CONFIG.SYS file must contain the statement:-

DEVICE = ANSI.SYS

You can use the line editor EDLIN to modify the CONFIG.SYS file in the root directory as follows where <CR> implies carriage return:-

Enter EDLIN CONFIG.SYS <CR>
Enter I <CR>
Enter DEVICE = ANSI.SYS <CR>
Press CTRL-C <CR>
Enter E <CR>

The CONFIG.SYS file is now prepared for MS-DOS to set the correct running environment for the PDSP Demonstrator. Refer to your PC manual for further details about EDLIN or the CONFIG.SYS file. Re-boot the PC Operating System before using the Demonstrator.

The PDSP Demonstrator is available NOW from Plessey Semiconductors.

PDSP Prototyping Kits

Plessey Semiconductors offer a one-stop route for solving high performance DSP Problems with a range of DSP kits. Plessey's Technical Support Group have created a range of five DSP kits. These contain all the PDSP devices needed to perform an extensive range of DSP Algorithms.

As complete units the PDSP Boxes contain all the devices, sockets, data sheets and application notes to build your own DSP system.

Additionally, all DSP Boxes contain the PDSP Demonstrator software, an IBM-PC compatible development system with device models that accurately replicate the functions of the real devices.

PDSP BOX 1

50ns FFT Butterfly Box & 20MHz Complex Arithmetic

- PDSP16112A BO AC x 1
- PDSP16318A BO LC x 2
- Plus Sockets
- 20MHz Complex Multiplier/Accumulator
- 50ns FFT Radix 2 DIT Butterfly
- 20MHz Complex Correlation/Convolution

PDSP BOX 2

40MHz Address Generation: 8 Through 64 Bit

- PDSP1601A BO LC x 1
- PDSP1601 BO LC x 1
- PDSP1640A BO LC x 2
- PDSP1640 BO LC x 2
- Plus Sockets
- 20MHz FFT Address Generation (In Place)
- 40MHz FFT Address Generation (Not In Place)
- 40MHz DMA Address Generation
- 40MHz FILTER Address Generation
- 40MHz Digital Waveform Synthesis
- 20MHz Variable Accuracy Barrel Shifting

PDSP BOX 3

Full Accuracy Complex Datapath FFTs & Complex MACs

- PDSP16116 BO AC x 1
- PDSP16318 BO LC x 2
- PDSP1601 BO LC x 2
- Plus Sockets
- 10MHz 16 x 16 Complex Multiply/32 Bit Accumulation
- 100ns Fully Automatic Block Floating Point Butterfly
- 10MHz FFT Address Generation (In Place)
- 10MHz Complex Correlation/Convolution

PDSP BOX 4

Pythagoras Box Coordinate Conversion & CMAC

- PDSP16330 BO LC x 1
- PDSP16112 BO AC x 1
- PDSP16318 BO LC x 1
- Plus Sockets
- 10MHz Cartesian to Polar Conversion
- 10MHz Complex Multiplier/Accumulator

PDSP BOX 5

FFT Support Box Power/Phase & Address Generation

- PDSP16330 BO LC x 1
- PDSP1601 BO LC x 1
- PDSP1640 BO LC x 2
- Plus Sockets
- 10MHz FFT Power/Phase Calculation
- 10MHz FFT Address Generation (In Place)
- 20MHz FFT Address Generation (Not In Place)
- 10MHz FFT Output Normalisation

Data Converters for Digital Signal Processing

Somewhere in your system you are almost certain to need to convert between the analog and digital domains.

Plessey has a whole range of data conversion ICs with performance from hundreds of Megahertz down to microsecond cycle times.

Typically video processing, whether for robotics, radar or any other imaging system, would use fast front end ADCs such as our eight bit SP94308 video system ADC or the simple but faster SP973T8. Still 8 bits, but with the possibility of oversampling for even greater accuracy is the 110MHz SP97508.

Perhaps you need to drive a graphics display at the back-end of your system or maybe you want to synthesise an analog waveform. Either way check our range of fast DACs which go up to 450MHz and include parts with graphics features.

Finally for servo control and mechanical measurement at lower speeds Plessey has a range of microprocessor compatible ADCs and DACs and a shaft encoder interface. Complete technical data for these products is contained in our Data Converters IC Handbook.

ANALOG TO DIGITAL CONVERTERS

Type	Function	Guaranteed Minimum Clock Rate	Process
SP97508	8-bit flash ADC	110MHz	Bipolar
SP9730E8	8-bit flash ADC, ECL outputs	30MHz	Bipolar
SP9730T8	8-bit flash ADC, TTL/CMOS outputs	30MHz	Bipolar
SP94308	8-bit video system ADC	20MHz	Bipolar

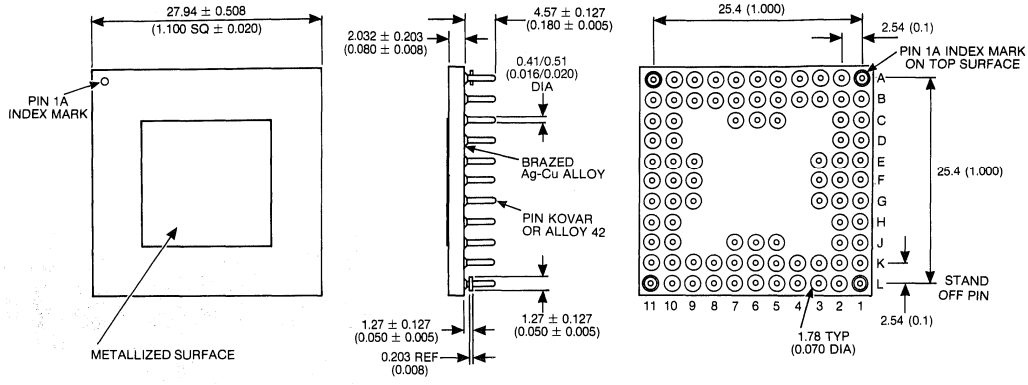
DIGITAL TO ANALOG CONVERTERS

Type	Function	Guaranteed Minimum Clock Rate	DAC Max Rise Time (10 % - 90 %)	Process
SP98608	8-bit multiplying DAC	450MHz	800ps	Bipolar
MV95308	8-bit video DAC	30MHz	6ns	CMOS
MV95408	8-bit video DAC	50MHz	5.5ns	CMOS
SP97618	8-bit graphics DAC	200MHz	1.1ns	Bipolar

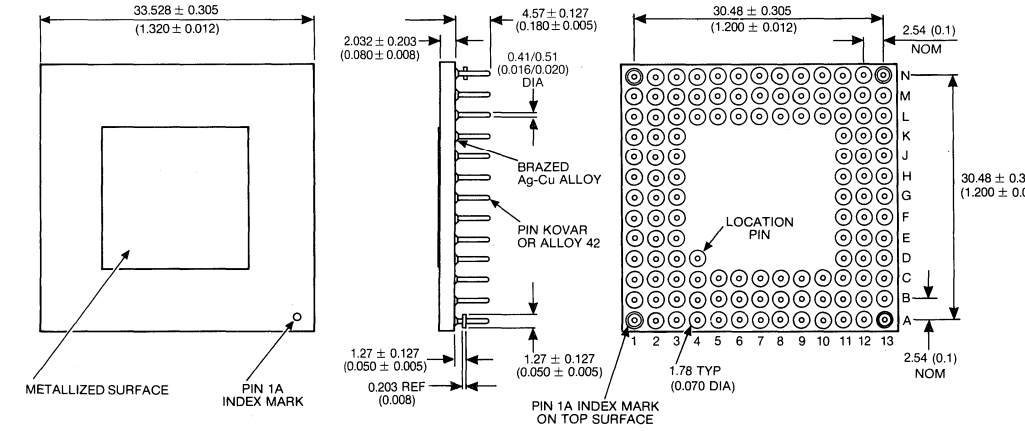
AUTOMATION

Type	Function	Frequency	Supply Voltage	Process
MV6101	Dual quadrature counter for shaft encoding applications	10MHz	5V	CMOS

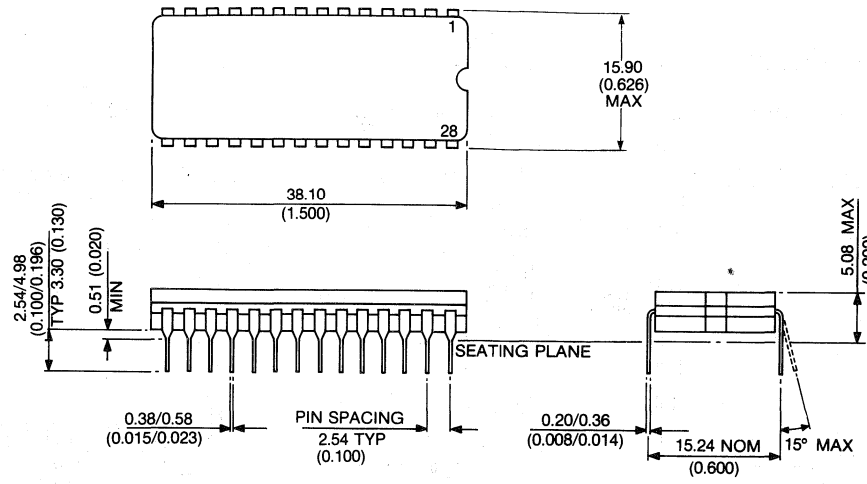
Package Outlines



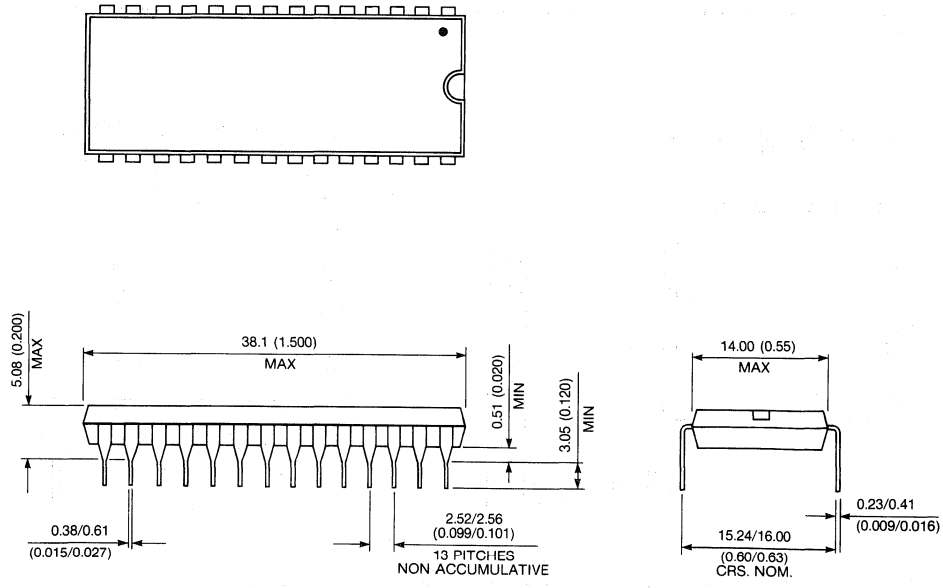
84-PIN GRID ARRAY PACKAGE — AC84



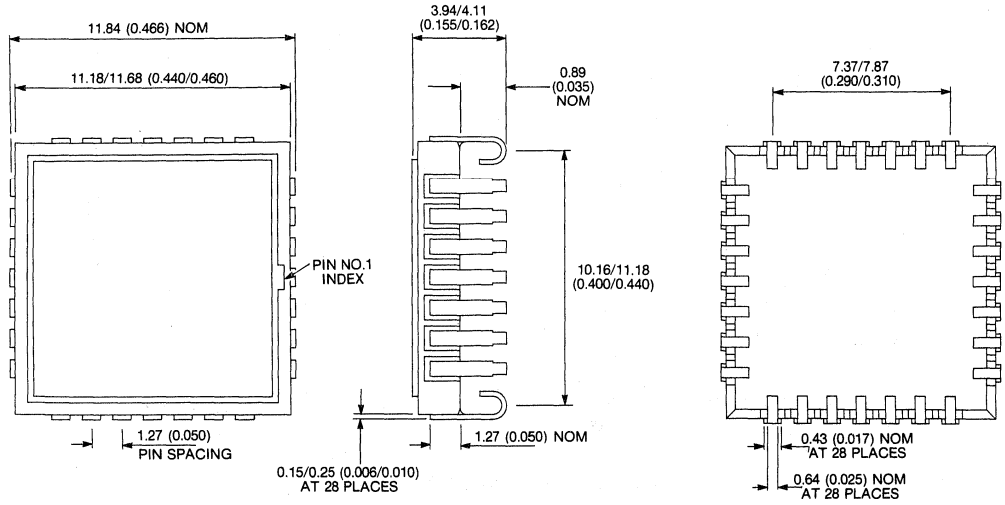
120-PIN GRID ARRAY PACKAGE — AC120



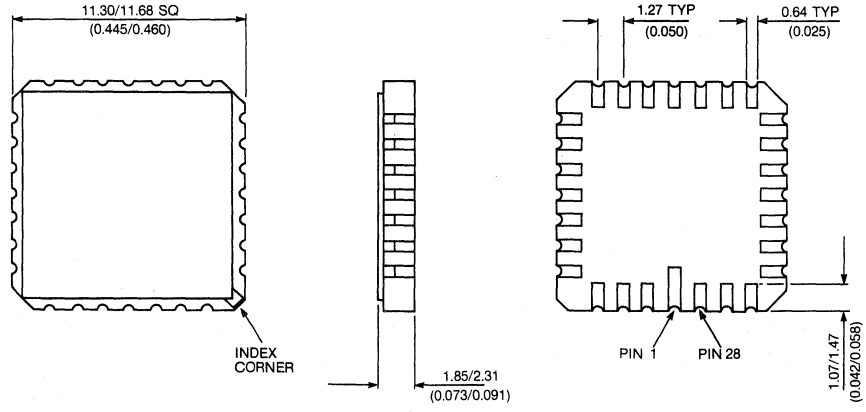
28-LEAD CERAMIC DIL - DG28



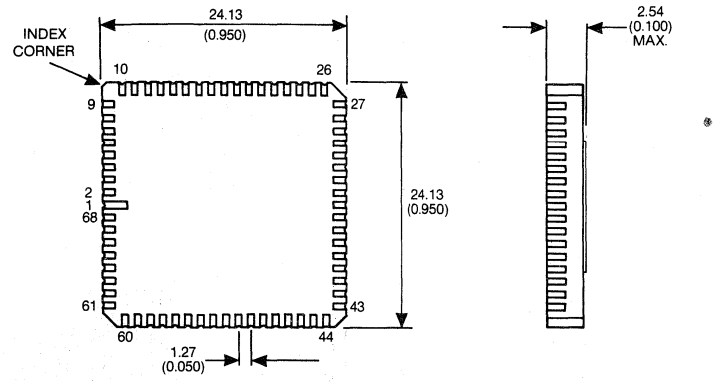
28-LEAD PLASTIC DIL - DP28



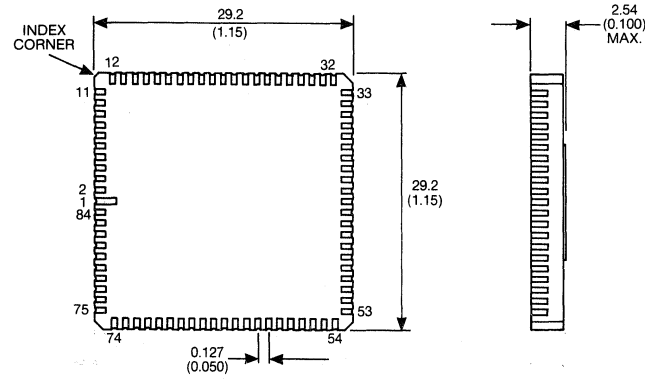
28-PIN LEADED CHIP CARRIER - HC28



28-PIN LEADLESS CHIP CARRIER - LC28
(HERMETIC)



68 CONTACT LCC PACKAGE — LC68



84-PIN LEADLESS CHIP CARRIER - LC84
(HERMETIC)

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Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
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API Elektronik Vertriebs GmbH, Augustinerring 27, D-8062 Markt Indersdorf. Tel: 08136/7092 Tx: 5270505 Fax: 08136/7398.
AS Electronic Vertriebs-GmbH, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Fax: 089 300 6001.
Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708. Fax: 07159/5119.
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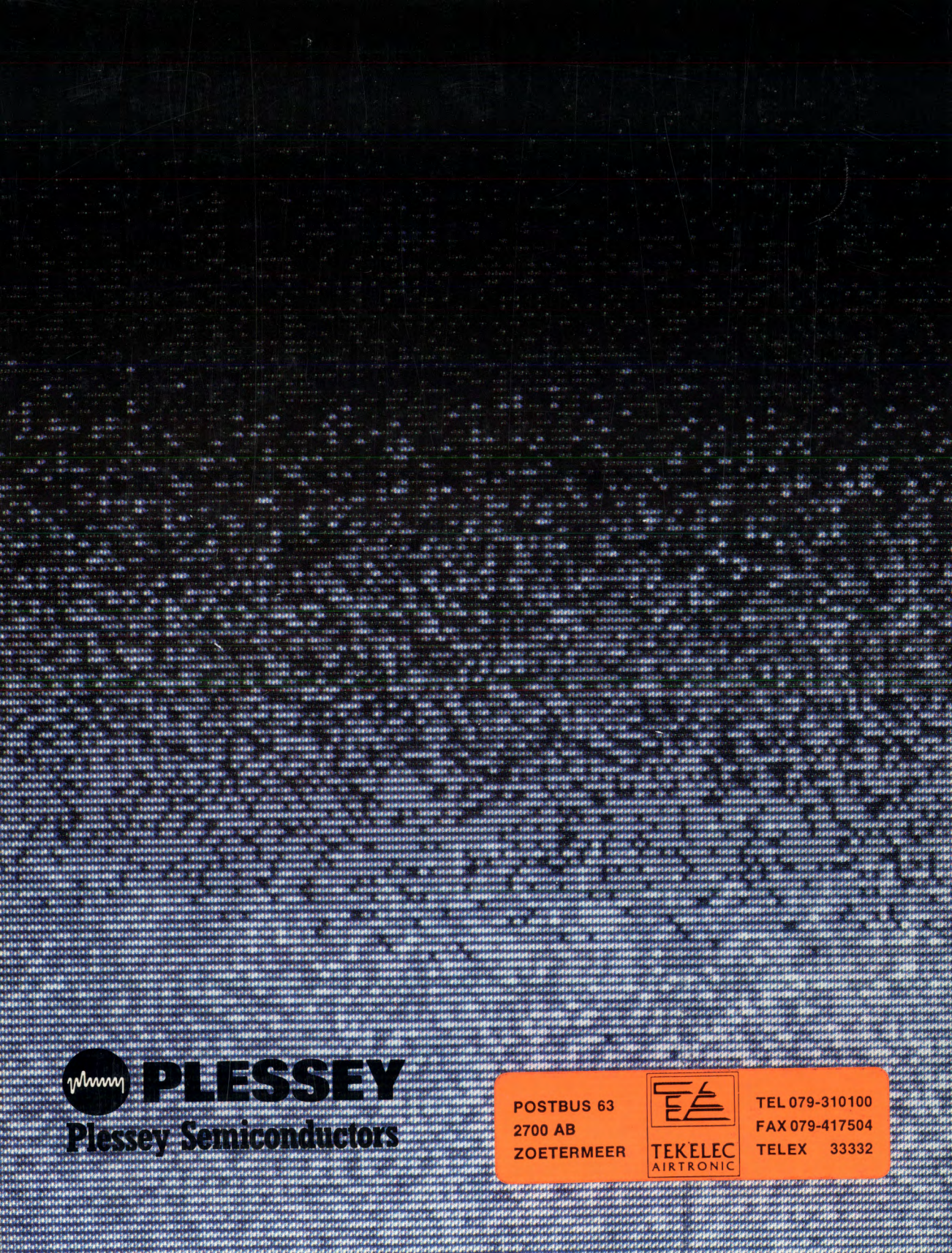
Publication No. P.S.2252 July 1988

PWC 2037/2047 7/88



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